YILDIZ TECHICAL UNIVERSITY
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A 4-GHz SiGe HBT DLL, CONFIGURABLE for SKEW CANCELLATION, MULTIPHASE CLOCKING AND FREQUENCY SYNTHESIZING APPLICATIONS

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TABLE OF CONTENTS

LIST OF SYMBOLS

A	Ampere
f	femto
F	farad
H	henry
G	Giga
g_m	Transconductance
Hz	Hertz
K	Kilo
K_{VCDL}	VCDL gain
K_{PD-CP}	Phase detector & charge pump gain
L	Length of transistor
m	mili
M	Mega
n	nano
p	pico
r_o	Output resistance
s	second
t_{ox}	Oxide thickness
μ	Micro
Uo	Mobility
V	Volt
W	Width of transistor
mW	mili-Watt
ζ	Damping factor
ω_n	Natural frequency
σ	standard deviation
σ^2	variance
Ω	Ohm

LIST OF ABBREVIATIONS

PLL	Phase-Locked Loop
DLL	Delay-Locked Loop
IC	Integrated Circuit
ADC	Analog/Digital Converter
CDR	Clock and Data Recovery
PSD	Power Spectral Density
CMRR	Common Mode Rejection Ratio
VCO	Voltage controlled oscillator
VCDL	Voltage controlled delay line
LP	Loop filter
LPF	Low pass filter
PD	Phase detector
PFD	Phase/Frequency detector
CP	Charge pump
SNR	Signal-to-noise ratio
SNDR	Signal-to-noise plus distortion ratio
ENOB	Effective number of bits
SFDR	Spurious free dynamic range
DNL	Differential non-linearity
INL	Integral non-linearity
EF	Emitter follower
PM	Phase Margin
ECL	Emitter Coupled Logic
ESD	Electrostatic Discharge
CML	Current Mode Logic
Gbps	Giga bits per second
Gsps	Giga samples per second
IEEE	The Institute of Electrical and Electronics Engineers, Inc.
I/O	Input/ output
LVDS	Low Voltage Differential Signalling
PCB	Printed Circuit Board
PSRR	Power Supply Rejection Ratio
V_{PP}	Volts peak-to-peak
BER	Bit Error Rate
MIM	Metal-insulator-metal
ISI	Intersymbol Interference

LIST OF FIGURES

PREFACE

First, I would like to thank my thesis advisor Prof. Dr. Atilla Ataman for his assistance and support during this work, and take a chance of working together within the future works hopefully.

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Finally I dedicate my thesis to my lovely family.

ABSTRACT

Synchronization and skew problems become more important as the modern electronic communication systems' operating frequencies increase. Delay Locked Loop (DLL), a first order feedback system, has been analyzed theoretically in comparable approach with PLLs and designed to operate at 4GHz and up to 6GHz clock signals for skew cancellation and multiphase clocking applications. In order to exploit DLLs' unique features, additional edge combiner circuitries have been designed in order to be able to synthesize up to 36GHz output clock signal.

Core DLL and additional circuitries are designed in 0.35μm SiGe HBT BiCMOS technology. High speed circuit techniques and high speed transistor fabrication techniques are investigated from noise features point of view, in order to lead excellent noise properties of DLLs to the edge. Thus, skew cancellation DLL output jitter is found to be 2.5ps peak-to-peak in analytical calculations (without edge combiners), and will be verified in prototype IC measurements.

Keywords: DLL, skew cancellation, frequency synthesizer, jitter, phase noise

JURY:

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2. Prof.Dr. Oruç BİLGİN Page: 150
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ÖZET

Modern elektronik haberleşme devrelerinin çalışma frekansları arttıkça, sekronizasyon ve istenmeyen saat işaret gecikmesi (skew) problemlerinin önemi artmaktadır. Senkronizasyon (skew cancallation) ve çok fazlı saat işareti kullanılan uygulamalarda kullanılmak üzere, birinci dereceden geribeslemli kontrol sistemi olan Gecikme Kilitlemeki Çevrim (DLL) devrelerinin teorik analizleri, Faz Kilitlemeli Çevrim (PLL) devreleriyle karşılaştırmalı olarak yapılmış ve 4GHz den 6GHz saat işareti frekanslarına kadar çalışabilecek şekilde tasarlanmıştır. Ayrıca DLL devrelerinin sağladığı avantajlardan sonuna kadar yaralanabilmek için 36GHz frekansına kadar ulaşabilen saat işaretlerini sentezleyen "kenar birleştirici (edge combiner)" devreler tasarlanmıştır.

Çekirdek DLL ve ek devreler 0.35μm SiGe HBT BiCMOS teknolojisi kullanılarak tasarlanmıştır. DLLlerin mükemmel gürültü özelliklerinin, sınırlarına kadar kullanılabilmesi için, yüksek hızlı devre teknikleri ve yüksek hızlı transistör üretim teknikleri, gürültü özellikleri bakımından incelenmiştir. Böylece, analitik hesaplamalarda, senkronizasyon için kullanılacak DLL'in çıkış titremesi tepeden tepeye 2.5ps olarak hesaplanmıştır ve bu sonuç prototip tümdevresinin ölçümleriyle doğrulanacaktır.

Anahtar Kelimeler: DLL, senkronizasyon, frekans sentezleyici, titreme, faz gürültüsü

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GENİŞLETİLMİŞ TÜRKÇE ÖZET

Son yıllarda, modern haberleşme elektroniği sistemlerinde veri iletim hızlarının ve dolayısıyla çalışma frekanslarının artması, verinin güvenilir hata oranlarında iletilmesi problemini doğurmaktadır. Düşük BER değerlerine erişebilme hedefi, yüksek frekanslı saat ve veri işaretlerinin gürültü özelliklerinin, alışageldik devre çözümlerinde elde edilebilenlere göre oldukça iyileştirilmesini gerekli kılmaktadır. Çoğunlukla mikroişlemciler, DSP ve sayısal devreler içerisinde istenmeyen gecikme problemlerinin üstesinden gelebilmek üzere kullanılagelen Gecikme Kilitlemeli Çevrim (Delay Locked Loop: DLL) yapılarının mükemmele yakın gürültü performansları, DLL yapılarının yüksek frekans bölgesinde çeşitli amaçlar için kullanılmasını gündeme getirmiştir.

DLL yapıları geri-beslemeli bir kontrol sistemidir. DLL, girişine uygulanan saat işaretini, gerilim kontrollü geciktirici hat (Voltage Controlled Delay Line: VCDL) yardımıyla geciktirmektedir ve ne kadar geciktireceği ise bir kontrol çevrimiyle belirlenmektedir. Geri besleme çevrimi, referans işaret ile VCDL çıkışındaki geciktirilmiş işaretin faz farklarının hesaplandığı faz dedektörü, hesaplanan faz farkı bilgisine göre VCDL'in kontrol işaretinin üretildiği yük pompası ve kontrol işareti üzerindeki yüksek frekanslı bileşenlerin süzüldüğü çevrim filtresinden oluşmaktadır [Bölüm-2 Şekil 2.1]. Yük pompasının kullanımı seçilecek faz dedektör topolojisine bağlıdır ve en genel halde DLL yapılarında kullanılmayabilir. DLL'de kilitlenme ise şu şekilde elde edilir; faz dedektörü herbir referans ve çıkış işaret periyodlarında yeni bir kıyaslama yaparak kontrol işaretinin bir sonraki değerini belirler iken, VCDL bu kontrol işaretine uygun yeni gecikme miktarını referans işaretine ekleyerek çıkış işaretini üretir. Böylece, kullanılan negatif geri besleme yardımıyla, VCDL'in çıkışındaki geciktirilmiş işaret yani DLL'in çıkış işareti ile giriş işareti yani referans arasında sıfır faz farkı elde edilmiş olur. DLL'in kilitlendiği durumda referans işareti ile çıkış işaretinin arasındaki faz farkının sıfır olması, tümdevre üzerinde saat işareti dağıtımı yapılırken farklı noktalarda ortaya çıkan istenmeyen gecikmelerin (skew) ortadan kaldırılmasında kullanılabileceğini göstermektedir. Bu istenmeyen gecikmeler, tümdevre üzerinde saat işaretinin dağıtılması esnasında farklı noktalara ulaşırken, eşit olmayan parazitik etkilere maruz kalması ve/veya eşit olmayan sayıda sürücü devreler kullanılması sonucu ortaya çıkabilmektedir. Bunların neticesinde istenmeyen gecikme değerleri büyük miktarlara ulaştığı takdirde, eşit yollar/sürücü sayısı gibi basit çözümler yetersiz kalmakta ve DLL gibi aktif devre çözümleri kaçınılmaz olmaktadır. DLL'in istenmeyen gecikmeleri ortadan kaldırması

sayesinde tümdevre üzerinde farklı noktalarda bulunabilecek, saat işareti kullanan devrelerin senkron çalışmaları sağlanabilecektir. Dolayısıyla DLL yapılarının en temel uygulama alanı, sayısal sistemlerde senkronizasyon ya da gecikme engelleme (skew cancellation) olarak ortaya çıkmaktadır.

DLL'de kilitlenmenin gerçekleştiği durumda yani giriş işareti ile çıkış işareti arasındaki faz farkı sıfır iken, pratikte VCDL'i oluşturacak devrelerin sıfır gecikme sağlayamayacağı hatırlandığında, toplam VCDL gecikmesi referans işaret periyodunun tam katları olmak zorundadır. Genel halde VCDL gerçeklenirken, minimum gecikmesi referans işaretinin bir periyodundan az tutularak ve ayarlanabilir gecikme miktarı ise referans işaretin en az bir periyodu olmak kaydıyla, kilitlenmenin sağlandığı durumda toplam VCDL gecikmesinin referans işaretinin bir periyodu kadar olması sağlanmaktadır. Pratikte VCDL'in tek bir birim devre ile gerçeklenmesi, istenilen ayarlanabilir gecikme miktarlarının (en az referans işaretin bir periyodu kadar) elde edilmesindeki zorluklardan ötürü mümkün olamamaktadır. Dolayısıyla VCDL birden çok geciktirici kat yardımıyla oluşturulur. Geciktirici katların özellikleri yukarıda belirtilen VCDL'in istenilen özelliklerine göre belirlenmelidir. DLL kilitlenmeyi, referans giriş işareti ile VCDL'de bulunan son katın çıkış işaretine göre sağladığından VCDL'i oluşturan herbir katın aynı miktarda gecikmeye sahip olması yanı eş olması, senkronizasyon için kullanılacak DLL yapılarında gerekli değildir. Ancak VCDL birbirlerine eş birim geciktirici katlardan oluşturulduğunda, DLL kilitlenmiş konumda iken, referans işaretin bir periyodu kadar olan VCDL'in toplam gecikmesi, herbir geciktirici kat çıkışında eşit olarak bölünmüş halde elde edilmiş olacaktır. Örnek olarak VCDL on adet geciktirici kat ile oluşturulduğunda, DLL kilitlendiğinde, herbir geciktirici kat çıkışında referans işaretin, on adet eşit faz farklarıyla ayrılmış halleri bulunacaktır. Bu eşit faz farkına sahip saat işaretleri, çok fazlı saat işaretine (multiphase clocking) ihtiyaç duyan özellikle zaman-paylaşımlı (time-interleaved) uygulamalar için kullanılabilmektedir. Ayrıca eşit gecikme değerleri ile bölmelenmiş referans saat işaretlerinin uygun şekilde birleştirilmesiyle (örneğin herbir geciktirici kat çıkış işaretlerinin yükselen kenarlarının birleştirilmesi), yüksek frekanslı saat işareti sentezlenebilmektedir. On adet geciktirici kat ile oluşturulan VCDL'in kullanıldığı DLL örneği için kilitlenmiş durumda, kenar birleştirici devrenin çıkışında referans işaret frekansının on katı frekansına sahip çıkış işareti üretilebilecektir. DLL'i oluşturan altblokların özellikleri ve DLL'in kullanım alanları ayrıntılarıyla bölüm-2'de açıklanmıştır.

Son yıllarda DLL yapılarının, özellikle GSM-1.8GHz sistemleri için yüksek frekans sentezleme uygulamalarında kullanıldığı ve gürültü özelliklerinin bu uygulamalar için incelendiği literatürde görülmektedir. DLL tabanlı frekans sentezleyicilerin, ring-osilatör kullanan PLL tabanlı frekans sentezleyicilere göre daha iyi gürültü özelliklerine sahip olmasının temel sebebi, titreme (jitter) olarak ortaya çıkan gürültünün, sürücü katların çevrim haline getirilmesiyle oluşturulan ring-osilatörde herbir saat işareti kenarında kümülatif olarak artması (jitter accumulation), DLL yapılarında ise ring-osilatör yerine kullanılan ve kaskad bağlı geciktirici katlardan oluşturulan VCDL'de gürültünün işarete herbir kat için bir kere eklenmesi ve döngü içerisinde kümülatif olarak eklenmemesidir. Dolayısıyla DLL tabanlı frekans sentezleyicileri, ring-osilatör kullanan PLL yapılarına göre daha düşük titremeye sahip yüksek frekanslı saat işaretinin üretilmesini sağlamaktadir. Ring-osilatörlerin kötü titreme performansının özellikle yüksek frekanslı saat işaretlerinin sentezlenmesinde kabul edilebilir sınırların dışına çıkması sebebiyle, PLLlerde LC osilatör kullanılması gerekli olmaktadır. LC osilatörlerin faz gürültüsü (phase noise) performansı rezonans tankında kullanılacak endüktans ve kapasite elemanlarının kalite faktörlerine (Q) doğrudan bağlıdır. İstenilen özelliklere sahip kapasite elemanlarının, günümüz üretim teknolojilerinde, tümdevre üzerinde gerçeklenmeleri mümkün iken, endüktans elemanlarının tümleştirilmesinde çeşitli sorunlar bulunmaktadır. Tümleşik endüktans elemanlarının büyük silikon alanı kaplaması ve tabana olan kaçak akımlar yüzünden ancak düşük kalite faktörlü olarak gerçeklenebilmesi, istenilen titreme/faz gürültüsü performansına ulaşılmasını zorlaştırmaktadır. Bu yüzden DLL tabanlı frekans sentezleyiciler, günümüzde ihtiyaç duyulan düşük titreme performansına sahip yüksek frekanslı saat işaretlerinin elde edilmesine olanak vermektedir.

DLL tabanlı frekans sentezleyicilerin, PLL tabanlı sentezleyicilere göre en önemli dezavantajı, frekans çarpma oranının VCDL'de kullanılan geciktirici kat sayısı tarafından belirlenmesidir. Kullanılacak geciktirici kat sayısının belirlenmesi esnasında, VCDL'den beklenen özellikler ve istenilen frekans çarpma oranı arasında bir çelişki bulunmaktadır. Pratik gerçeklemelerde geciktirici kat sayısı en fazla yüz adete ulaşabilmektedir ancak çalışma frekansları daha da arttığında bu sayı ancak on adet mertebelerindedir. Oysa PLLler oldukça yüksek frekans çarpma oranlarına ulaşabilmektedir. Bu özellikleri sebebiyle PLLler referans işareti olarak, düşük frekanslı ancak oldukça iyi gürültü özelliklerine sahip kristalleri kullanabilmektedir. DLLlerde ise kristallerden daha yüksek frekanslı referans saat işaretinin kullanılması zorunluluğu, daha gürültülü olan referans işaretinin çıkış işareti üzerindeki etkilerinin mümkün olduğunca küçük tutulmasını gerekli kılmaktadır. Aksi takdirde DLLlerin

mükemmel olarak nitelendirilebilecek gürültü özelliklerinin avantajları kaybedilmiş olacaktır. DLLlerin kendi iç gürültüsünün ve referans işaretindeki gürültünün çıkış işaretine etkileri bölüm-3'te incelenmiştir.

Yüksek performanslı tümdevrelerde, istenmeyen gecikmeler (skew) ve senkronizasyon sorunları, çalışma frekansları gigahertz ve üzerine çıktıkça daha da büyük sorun teşkil etmektedir. Bu çalışma frekansı mertebelerinde, işaret iletim hatlarının parazitik direnç ve kapasite etkilerinin yanısıra parazitik endüktans etkileri de ortaya çıkmaktadır. Dolayısıyla düşük frekans uygulamalarında göz ardı edilebilen bir kısım parazitik etkiler ya da birinci dereceden parazitik eleman modellerine dayalı olarak geliştirilen çözüm önerileri (serim teknikleriyle eş uzunluktaki yollar ve/veya saat işareti dağıtım mimarileri gibi), gigahertz üzerindeki çalışma frekanslarında yeterli olamamaktadır. Dolayısıyla işaret hatlarının parazitik etkilerinin dağılmış olarak modellenmesi ve düşük gürültü özelliklerine sahip aktif devreler yardımıyla senkronizasyonun sağlanması zorunluluk olmaktadır. Bu aktif devreler PLL veya DLL olmalıdır ancak PLLlerin kötü gürültü performansı sebebiyle DLL tercih edilmelidir.

Yapılan çalışma 4GHz frekansındaki saat işaretleriyle çalışacak ve senkronizasyon amacıyla kullanılacak bir DLL tasarımıdır. Bölüm-2'de anlatılan DLL altbloklarının özellikleri, bölüm-3'te açıklanan sistem seviyesi kararlılık ve gürültü performansı uyarınca sistem tasarlanmıştır. Faz karşılaştırıcı olarak ölü-bölgesi (dead-zone) olmayan Faz/Frekans Dedektörü, yeni bir yük pompası ve buna bağlı çevrim filtresi ile oniki adet geciktirici kattan oluşan VCDL tasarlanmıştır. VCDL'i oluşturan geciktirici katların gecikme ayarı, herbir katın çıkışındaki kapasitif yükün, ayarlı kapasite elemanı olan varaktörler ile belirlenmesi sağlanarak yapılmaktadır. DLL'in gürültü duyarlılığını azaltmak üzere, sistemde yer alan bloklar diferansiyel işaretler ile çalışacak biçimde tasarlanmıştır. Bunun tek istisnası, VCDL'de yer alan varaktör elemanlarının tek uçlu kontrol gerilimine ihtiyaç duymaları sebebiyle, çevrim filtresinin çıkışında oluşturulan diferansiyel kontrol işareti, tek uçlu hale dönüştürülmesidir.

Bölüm-4'te DLL'i oluşturan herbir altbloğun tasarımlarının yanısıra DLL sisteminin bir araya getirilmesi, yapılan serim sonrası simulasyon sonuçlarıyla birlikte anlatılmaktadır. DLL, PVT (Process, Voltage, Temperature) saçılım köşe durumlarında çalışacak şekilde tasarlanmıştır. Proses saçılmaları uç koşulları üretici firmadan alınmış (yüksek hız, düşük hız, yüksek β, düşük β durumlarının ikili kombinasyonları), besleme gerilimi uç noktaları 3V-3.6V ve çalışma sıcaklık aralığı -20°C ile +130°C olarak seçilmiştir. İlgili bölümün sonuç kısmında, tasarımı tamamlanan DLL'in fonksiyonelliği, kararlılık ve gürültü performansları gerek serim

sonrası simulasyon sonuçları gerekse analitik hesaplama neticileri ile sunulmuştur. Ayıca DLL içerisinde kullanılan herbir kutuplama akım kaynağının referansları, band-aralığı referansından faydalanarak PVT değişimlerinden en az etkilenecek biçimde üreten bir kutuplama merkezinden sağlanmaktadır. Bu birim, ayrıca tasarlanan test bloklarıyla birlikte bölüm-5'te ele alınmaktadır.

Tasarlanan 4GHz frekansında çalışan DLL'den, frekans sentezleyici ve çok fazlı saat işareti üretici olarak da araştırma amaçlı faydalanabilmek için VCDL'i oluşturan geciktirici katlara ek özellikler ilave edilmiştir. Dolayısıyla tasarımda güç harcaması birinci etken olarak göz önüne alınmamıştır. Özellikle frekans sentezleyici olarak DLL'in ve kenar birleştirici olarak çalışabilecek farklı devre yapılarının performanslarının kıyaslanabilmesi için iki adet kenar birleştirici yapı da test amaçlı tasarlanmıştır. VCDL ile kenar birleştirici bloklar arasına tamponlar eklenerek, DLL'in ek test bloklarından en az seviyede etkilenmesine çalışılmıştır. Ayrıca DLL'in 6GHz'e kadar güvenilir çalışması sağlanarak, frekans çarpıcı konfigürasyonunda çıkış işaret frekansının 4GHz×5 ile 6GHz×6 aralığında ayarlanabilir olması sağlanmıştır. Çarpma faktörü olan 5 veya 6'nın seçimi, yüksek performanslı bir multiplexer yardımıyla geri-besleme noktasının belirlenmesiyle sağlanmaktadır. Ancak elde edilen en yüksek 36GHz civarındaki çıkış işaretlerinin kuvvetlendirilmesi ve tümdevre dışarısına alınmasında, özellikle bağlantı adalarının (bonding pad) ve seçilecek paketin bandgenişliği sınırlamaları sebebiyle sorun bulunmaktadır. Bu sorunların üstesinden gelebilmek üzere eş zamanlı olarak, endüktif olarak bandgenişliği arttırılan (inductive peaking) çıkış sürücü katın tasarımı, uygun genişbandlı ESD korumalı bağlantı adası tasarımı ve yüksek frekanslarda çalışmaya uygun paket seçimi çalışmaları devam etmektedir. Ayrıca bahsi geçen frekans bölgesinde çalışmaya müsait ölçü aletlerinin temin olanaklarına göre, yine tasarlanan çıkış katının sürdüğü, tümdevre üzerine yerleştirilecek RF-pad yardımıyla çıkışların, "RF Probe Station" aracılığıyla gözlenmesine çalışılacaktır. Frekans sentezleme çalışmalarının amacı 40Gbps optik haberleşme standardına uygun saat işaretleri üretebilmektir. Bölüm-2.5'te anlatılan, DLL'in farklı uygulama alanlarında sağlaması gereken performans kriterleri hesaba katılarak, bahsi geçen çözümlerden hangisinin veya hangilerinin seçileceğine karar verilecek ve prototip tümdevresi son haline getirilecektir. Ayrıca DLL'in çevrim bandgenişliğinin gürültü performansına etkilerini gözlemleyebilmek amacıyla, çevrim filtresini oluşturan kapasite elemanı ve yük pompası kuyruk akımı değerleri prototip tümdevre dışarısından kontrol edilebilir hale getirilmiştir. DLL'e ek test devreleri detaylı olarak bölüm-5'te anlatılmıştır.

DLL seriminin tamamlanmış olmasına rağmen, bahsi geçen test bloklarının çıkışlarında yer alacak sürücü devre çözümleri ve paket seçimi üzerinde yapılan çalışmaların halen devam etmesi ve izin verilen silikon alanının henüz belirli olmaması sebebiyle, prototip tümdevresinin üst seviye birleşimi henüz tamamlanamamıştır. DLL'i oluşturan blokların seriminde, simetri önplanda tutulurken, yüksek frekanslı işaret taşıyan hatlar arasında kuplaj en az seviyeye indirgenmeye çalışılmıştır. Önemli bir diğer husus ise, tümdevre üzerindeki sıcaklık gradyanı olduğundan, herbir altblok kendi içerisinde $1W/1mm^2$ oranı uyarınca serilmiştir. Besleme ve taban zıplaması (V_{DD}/Ground Bounce) olarak, devrelerin kuyruk akımlarını anahtarlaması sebebiyle ortaya çıkan gürültüden sistemin en az seviyede etkilenmesi için herbir alt devre için besleme akım çevrimini en kısa yapacak biçimde beslemeler arasında kuplaj kapasiteleri kullanılmıştır. Ayrıca besleme hatları herbir metal katmanda dağıtılarak, beslemeler arası parazitik kapasitesinin arttırılmasına çalışılmıştır. Diferansiyel işaret hatları, ortak işaret eşitliğini muhafaza etmek üzere uçları arasındaki kuplaj arttırılacak biçimde mesafelendirilirken, tabana yaptıkları parazitik kapasite ve hatların kendi parazitik dirençleri en aza indirilmeye çalışılmıştır. Bu amaçla dört adet metal katmana sahip prosesin en üst metal katmanı beslemelere ayrılmış, yüksek frekanslı saat işareti bir alt seviye olan metal-3 katmanından taşınmıştır. Metal-1 ve metal-2 katmanları ise alt blokların iç bağlantıları ile beslemelerinde kullanılmıştır. Özellikle üst seviye birleşim yapılırken, uzun hatların sonlarında yer alan emetör izleyici devrelerin, uzun hatların olası büyük parazitik dirençleri sebebiyle çınlama yapmaları engellenmeye çalışılmaktadır. Besleme hat genişlikleri, hatlardan çekilen akım değerleri uyarınca arttırılarak ve simetrik dağıtılarak, beslemelerde oluşacak parazitik I×R düşmesi en aza indirgenecektir.

DLL'in gürültü performansını büyük ölçüde belirleyen blok olduğundan, tek başına bir VCDL ürettirilmiştir. Test amaçlı olan ve DLL çevrimi içerisinde bulunmayan oniki katlı bir VCDL ve aynı VCDL'in ring-osilatör konfigürasyonu, tasarımda kullanılan 0.35μm SiGe BiCMOS prosesin önceli bipolar eşleniğinde ürettirilmiştir. VCDL, gürültü özelliklerinin ölçülebilmesi, ring-osilatör konfigürasyonu ise kontrol gerilimi ile çıkış frekansının değişiminden faydalanılarak, VCDL'in gecikme kontrol karakteristiği dolaylı olarak ölçülebilmesi amaçlarıyla ürettirilmişlerdir. Yardımcı ring-osilatör konfigürasyonun gürültü mekanizması VCDL'den farklı olduğundan, VCDL gürültü karakteristiğinin çıkartımına yardımcı olamayacaktır. Bu blokların çeşitli ölçüm düzenekleri ile karakterize edilmesi, hazırlanmakta olan prototip tümdevresi için önemli ölçüde yararlı olacaktır. Bu iki bloğun ölçüm çalışmaları halen devam etmektedir ve bölüm-5'te açıklanmıştır.

1 INTRODUCTION

1.1 Motivation

Delay Locked Loops (DLLs) become more popular circuit technique in modern electronic communication systems. As the name of DLL itself suggests, it is a feedback system that controls the delay of the ingoing signal and locks its output to the input with a constant amount of phase difference (usually zero) that allows eliminating the unwanted phase differences ("skew") in synchronizing signals, such as clock signal, and circuits those using clock signals, would work synchronized with each other, which is called "skew cancellation". This feature makes the DLLs' main application area, synchronization of dynamic digital circuits, in DSP (Digital Signal Processing) chipsets and microprocessors. Phase Locked Loops (PLLs) are also commonly used in this manner [Johnson, M. and Hudson, E., 1988], but higher noise immunity, inherently stable nature and so easier implementation of DLLs with respect to the PLLs make them more attractive in skew cancellation applications [Liu, A. and Lee, J., 1999].

Well known circuit techniques could be applicable to DLLs working on clock signals at megahertz frequency range, either in skew cancellation or frequency multiplication or clock/data recovery (CDR) or time-to-digital converter or symbol synchronization applications. Last couple of years, researches have been focused on exploiting DLLs' noise properties in some applications with different circuit techniques and DLLs working on hundreds of megahertz's had been demonstrated.

In mixed signal applications such as data converters, in addition to the skew cancellation, multiphase clocking (not only quadrature clock signals) allows paralleling the processes. Especially, Time-Interleaving topologies which have equal or more than 2 ways are widely used in low/moderate resolution and high speed Analog-to-Digital Converters (ADCs) which accommodate samplers (Sample&Hold or Trach&Hold circuits) requiring low jitter evenly spaced clock signals.

Transceivers in communications electronics generally use PLL based local oscillators (LOs), containing ring oscillator VCO or less noisy LC VCO [Razavi, B., 1998]. But increasing demand in higher carrier frequencies in newer applications, either wired or wireless, tightens the phase noise specification of the LOs. Excellent phase noise behavior of DLLs with respect

to the ring oscillator PLLs could make them major LO topology in a couple of years although its' low frequency multiplication factor. Frequency synthesizer DLLs, mainly accommodate a core DLL working on hundreds of megahertz range and different kinds of frequency synthesizer "Edge Combiner" circuitries with the output frequency up to 1.8 GHz for GSM applications [Chien, 2000], [Foley, D. and Flynn, M., 2000] and also a modified version of DLLs as a frequency synthesizer, called re-circulating DLLs [Ramin, F. and Dally, W., 2002] which could be considered as a combined version of DLLs and ring oscillator PLLs, had been demonstrated.

1.2 Goals

Skew canceller DLLs operating at low frequencies and frequency synthesizer DLLs operates at higher frequencies, implemented in modern CMOS technologies, had a core DLL working on up to a couple of hundred megahertz had been demonstrated. Also DLLs producing multiphase clock signals for over giga sample per second time-interleaved ADCs working on same frequency range (a couple of hundred megahertz) could be seen on some products such as high speed sampling oscillators.

Clock distribution on modern ICs could be problematic while dealing with over a few megahertz clock signals. Some layout techniques for clock distribution such as H-tree mainly rely on achieving almost same amount of line length so each clock line sees almost same parasitic line resistances and capacitances although these lines take place in different portions of the IC. As the clock frequency increases, distributed behavior of parasitic elements and parasitic line inductances could be problematic and low timing budgets for synchronization at higher frequencies makes basic layout techniques incapable of solving skew phenomenon. Especially distribution of the over gigahertz range clock signals and synchronization of some even cascaded circuit blocks is a challenging matter.

Wired 10Gbps - 50Gbps communication systems, using laser pulses or stand-alone LC oscillator clock sources, require high speed circuit techniques (such as interleaving, downsampling) and/or high speed devices such as SiGe, GaAs, InP HBTs and HEMTs. Clock generation for these applications is another challenging matter and so frequency multiplication techniques using DLL and circuit techniques dealing with those high frequencies should be developed, designed and carefully characterized in order to compare different frequency synthesizer solutions.

This work focuses on "A 4GHz DLL Implementation" which could be mainly used as a skew canceller. DLL also could produce 6 evenly spaced 4GHz clock signals, which could be used in a 6 way Time-Interleaved ADC resulting equivalent sampling rate of 20-25Gsps. DLL design is based on 0.35μm SiGe HBT BiCMOS process parameters. After designing the 4 GHz DLL, two different edge combiner implementation approach (LC tank and OR/AND logic) for frequency multiplication techniques are investigated and designed in order to compare them. High speed circuit techniques for MOS and HBT devices were also investigated throughout the work in order to deal with up to 30GHz clock signals.

1.3 Thesis Organization

The goal of the thesis is to review the theory of PLLs and DLLs, design and analysis of DLL circuits and a complete implementation of 4GHz SiGe HBT DLL for Skew Cancellation and Multiphase Clocking and also investigation of frequency synthesis of 20GHz-30GHz clock signals.

Chapter 2 presents basic description of DLLs and its loop components. Also this chapter gives some examples of DLL application areas and discusses over gigahertz range ICs system design problems.

Chapter 3 explains both s-domain and z-domain DLL models in order to describe the loop dynamics and noise behavior of DLLs.

Chapter 4 is the major subject of the thesis. A 4GHz SiGe HBT DLL design strategies, design steps, simulation results of the system will be presented.

Chapter 5 deals with the implementation problems, additional test circuits and measurement.

2 DLL BASICS AND LOOP COMPONENTS

Delay locked loop is a feedback system that produces an output signal with zero phase difference with respect to its reference signal. DLL has three basic components (Figure 2.1);

1. A phase detector,

2. A loop filter,

3. A voltage controlled delay line.

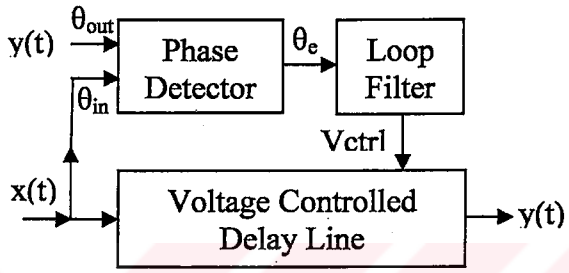


Figure 2.1 Basic DLL block diagram.

The phase detector compares the phase of the input signal, x(t), against the phase of the VCDL output signal, y(t). Output of the phase detector is a voltage proportional to the phase difference between its two inputs. The loop is considered "locked" if the phase difference is constant with time. The loop filter filters out the phase difference voltage at the phase detector output. Loop filter is a lowpass filter, which suppresses the high frequency signal components and noise. Output of the loop filter is applied to the VCDL as the control voltage, Vctrl. This control voltage changes the delay of the VCDL in a direction that reduces the phase difference between the input signal, x(t), and the output signal, y(t). When the loop is locked, the control voltage is such that the output phase of the VCDL is exactly equal to the phase of the input signal; however, there may be a static phase error present. This error tends to be small in a well-designed loop.

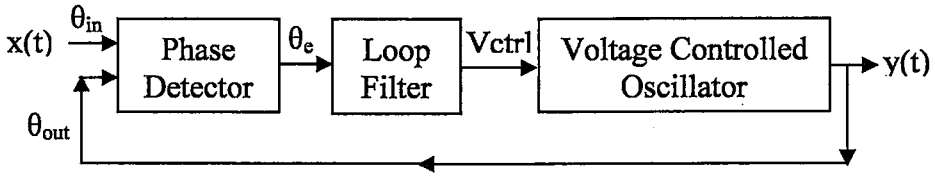


Figure 2.2 Basic PLL block diagram.

DLLs generally built up with same building blocks of PLLs as shown in Figure 2.2 , but one major component, that is; voltage controlled oscillator (VCO) used in PLLs is replaced with voltage controlled delay line (VCDL). VCOs of PLLs oscillate in a predetermined frequency range. Oscillator output frequency is adjusted according to the phase and/or frequency difference with respect to the reference signal and the loop locks this output signal to the reference input. In DLLs, the loop locks reference input signals phase to its delayed versions phase at the output of the VCDL. PLL's output frequency need not to be the same as the reference input frequency because built in VCO can oscillate at a higher frequency with respect to the reference. In this case, frequency dividers could take place in feedback path of PLLs to reduce the VCO output frequency to the same value that of the reference in order to make a comparison. This makes PLL attractive in frequency synthesizers because large multiplication ratios could be achieved by the aid of frequency dividers. But VCDLs in DLLs just buffer its input to the output, with controllable phase difference. So the reference input and output of DLL are at the same frequency. But if VCDL is constructed with equal delay stages, it contains equally divided phases of the one period of reference signal, which gives an opportunity for multiplication, by properly combining these different phases of the reference signal. Naturally, the number of delay stages used in VCDL directly determines multiplication ratio and of course unequal delay stages or different implementation methodologies (such as passive, T-line) in VCDL could prevent frequency multiplication.

Loop components of DLL are almost same as those of PLLs. But it is important to keep in mind that PLL based frequency synthesizers generally consist of frequency dividers so PLL's comparison frequency at the inputs of the phase detector is much lower than the output frequency. This attribute makes loop components in PLLs, except VCO, easier to implement with well known circuit techniques with desired characteristics. In contrast, DLL loop components has to work properly at much higher frequencies, cause of the nature of the DLL that the input and the output frequencies are the same.

There are different kinds of loop components which should be carefully chosen whose characteristics could be useful in different applications of DLLs and PLLs. Some major kinds of loop components and circuit techniques will be described briefly in following sections.

2.1 Phase Detectors

Phase detector is a kind of comparator produces a DC output error signal, $\theta_e=\theta_{in}-\theta_{out}$, corresponding to the phase difference of the two inputs. Output of the phase detector could be written as;

$$v_e=K_{PD}.\theta_e \tag{2.1}$$

Where v_e is the DC output voltage, θ_e is the phase difference between the input signals and K_{PD} is the phase-detector gain in volts per radian, V/rad. According to this definition, phase detector characteristic is linear in ideal case as shown in Figure 2.3. However, in practice the response of a phase-detector is generally nonlinear and repeats in a cyclic fashion over a limited phase range. The response is usually almost linear within a narrow phase difference range close to the point at which the loop will normally lock, and the slope of the characteristic, the phase-detector gain K_{PD}, is of most interest at this point.

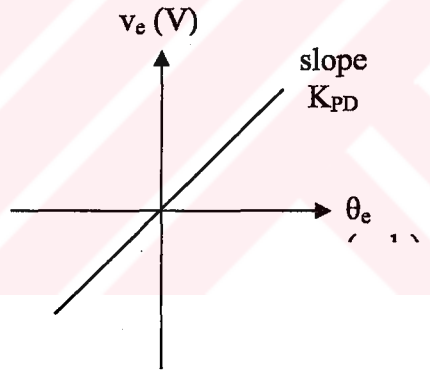


Figure 2.3 Phase detector characteristic in ideal case.

Phase detectors could be examined in two basic categories; multiplier type phase detectors and sequential phase detectors.

2.1.1 Multiplier Type Phase Detectors

Multiplier type phase detectors could be understood as a basic analog multiplier. If the two input signal of the multiplier considered as sinusoids, $x_1(t)=A_1.\cos(\omega_1 t+\theta_1)$ and $x_2(t)=A_2.\cos(\omega_2 t+\theta_2)$, the output of the multiplier $v_e(t)=K.x_1(t).x_2(t)$ could be arranged as follows with aid of trigonometric manipulations;

$$v_e(t)=[\cos\{(\omega_1-\omega_2)t+(\theta_1-\theta_2)\}+\cos\{(\omega_1+\omega_2)t+(\theta_1+\theta_2)\}]K.A_1.A_2/2 \tag{2.2}$$

where K is proportionality constant. It is clear that multiplier produces two frequency tones, difference and sum of input signals. In DLLs the two input signal of the phase detector has the same frequencies so first term of equation (2.2) became time invariant. The loop filter could filter out the second term of equation (2.2), which is at the summed frequency. And the output of the phase detector becomes proportional to the phase differences of the two input, recalling $\theta_e=\theta_1-\theta_2$;

$$v_e(t)=\cos(\theta_e).K.A_1.A_2/2 \tag{2.3}$$

Equation suggests that the phase-detector output varies sinusoidally with phase difference, with zeros at $\theta_e=\pi/2+n.\pi$ as shown in Figure 2.4. For zero error voltage, which means that the loop is locked, cosine term should be zero. This corresponds to $\theta_e=\theta_1-\theta_2=90^o$ phase difference, so multiplier type phase detectors has a static phase error of 90^o in locked condition. From equation (2.3), adjusting the cosine term $\cos(\pi/2-\theta_e)$, phase detector gain could be written as

$$K_{PD}=-K.A_1.A_2/2 \tag{2.4}$$

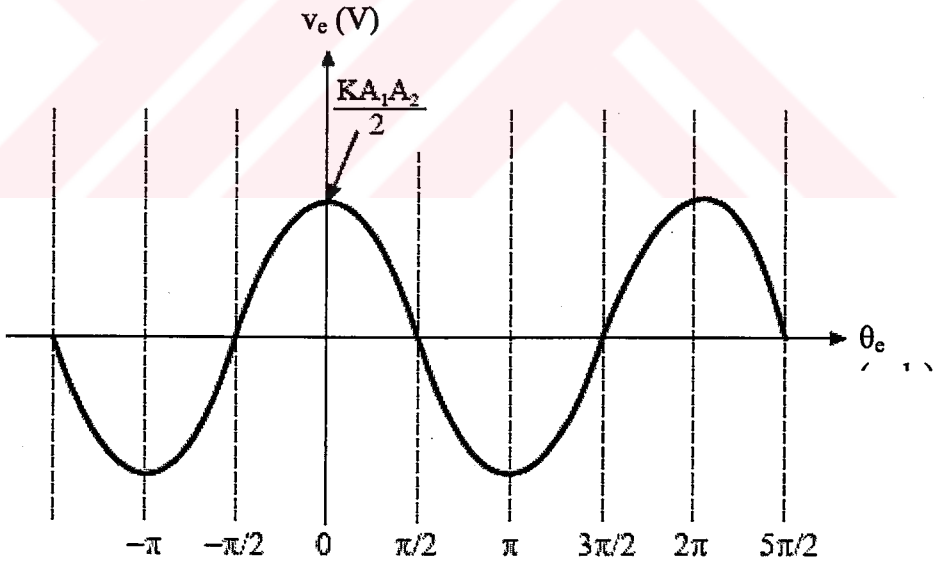


Figure 2.4 Analog multiplier phase detector characteristic for sinusoidal inputs.

This types of phase detector could be useful in noise environments, because unwanted parts of the output signal could be removed and detector has no need to reference or threshold values which could be affected by the noise and degrades detection performance. Depending on the circuit topology, SNR values down to 10dB does not make the circuit malfunctions.

Phase detector exhibits a variable voltage slope and is monotonic. The phase detector gain is zero when the phase difference is zero, and is greatest when the input phase difference is 90°. Hence, to maximize the useful phase detection range, the loop should be arranged to lock to a phase difference of 90°. For this reason, a multiplier type phase detector is often called a quadrature phase-detector. Thus, although the phase difference is 90° in an ideal quadrature loop, the phase error is considered to be zero. The useable range of the detector, where the operation is approximately linear, is limited to within $\pm\pi/4$ radians of θ_e. So, the phase detector range is $\pi/2$. As could be seen from equation (2.4) phase detector gain is depended on input signal amplitudes, which is an undesirable attribute resulting input depended loop dynamics in DLL.

If one of the input signals of multiplier phase detector is square-wave rather than sinusoidal, linearity will improve and if both of the inputs are square-wave, besides linearity also capture range will increased too. But loop could react to the odd harmonics of the squared-wave at the inputs resulting false locking. In these situations, static phase error and input amplitude dependent gain are again problematic. Besides, linearity is strongly dependent on %50 duty cycle of the input signals. Further analysis about multiplier phase detectors could be found in [Pak, B., 2002]

Gilbert Cell and XOR phase detectors are well-known multiplier type phase detectors.

2.1.2 Sequential Type Phase Detectors

Sequential type phase detectors operate only on the transitions of the input signals and therefore implemented in digital form. The sequential type poorly operates under low S/N conditions in which they exhibit a threshold effect. So, they are generally used at S/N ratios above 10dB. However, they can offer far superior capture and tracking performance. They can provide zero phase difference (or 180°) in locked condition and a constant gain over the entire operating range. Since they operate on the rising or falling edge, but not both, the phase-detector output has a ripple at the input frequency, which is difficult to suppress, and undesirable. However, operating only on one edge of the input signal makes the phase-detector characteristic independent of the duty cycle.

An important property of the sequential phase-detectors is; they produce a DC output even if the input signal frequencies are different, whereas multiplier phase detectors do not. Therefore, they also provide information about the magnitude of the frequency error.

However being sensitive to edge transitions, a sequential phase-detector will misinterpret a missing edge as a frequency error and the loop will be forced to correct this error. So, they do not have the ability to flywheel. This behavior can be modified significantly. Sequential phase detectors can also be shown to produce harmonic lock voltages, but it is more difficult to generalize about sequential operations. However, tracing the waveforms of any specific sequential PD will quickly show its harmonic locking properties.

The simplest sequential phase detector is the set-reset (SR) flip-flop (Figure 2.5a). The flip-flop is set on the rising (or falling) edge of input-1 and is reset on the rising edge of input-2 as shown in Figure 2.5b. The ripple frequency is equal to the input frequency.

The mean DC output varies linearly between logic-0, when θ_e=0 rad, and logic-1, when $\theta e=2\pi$ rads. The characteristic is plotted in Figure 2.6. This is the case for typical CMOS implementation, where the output swings from rail-to-rail, ground to VDD. The characteristic is sawtooth rather than triangular. In order to achieve a symmetrical output voltage swing, a DLL incorporating this phase-detector would lock at a phase difference of π rads. However, the DC offset of VDD/2 should be introduced at the loop-filter for the DLL to operate correctly. This phase-detector has a linear range of 2π rads, which is twice that of an XOR phase-detector. So, it has an improved capture and tracking capabilities. The phase-detector gain is:

$$K_{PD}=V_{DD}/2\pi \qquad (2.5)$$

The foregoing analysis assumes that the flip-flop responds equally fast to set and reset inputs. Any speed difference results in a static phase error. As a result something other than 180° phase difference is necessary to obtain an average output of VDD/2, if the set and reset operations take place at different speeds. Considering the typical SR flip-flop implementation in Figure 2.5a, this circuit has faster response to the reset than to the set input. Therefore, it is not appropriate for applications in which a small static phase error is important. Also, in the absence of an input signal the mean output latches-up in one state, preventing the detector from being used in CDR applications.

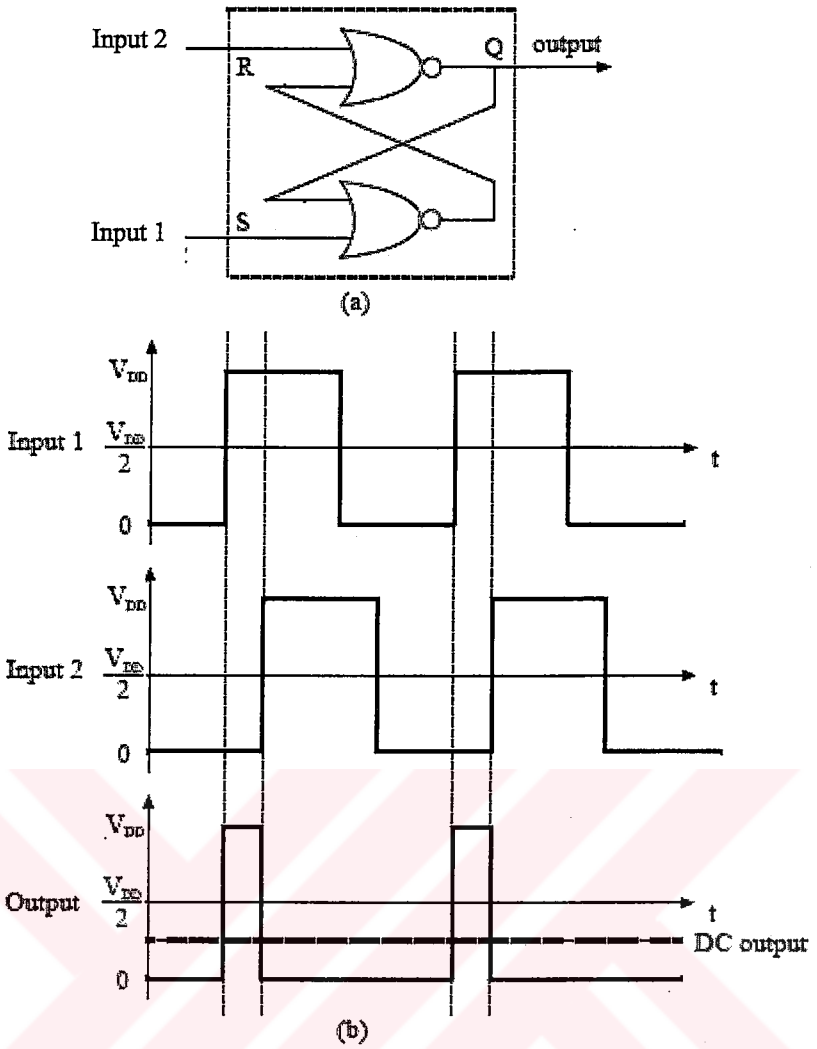


Figure 2.5 (a)SR flip-flop phase detector (b) SR flip-flop phase detector operation.

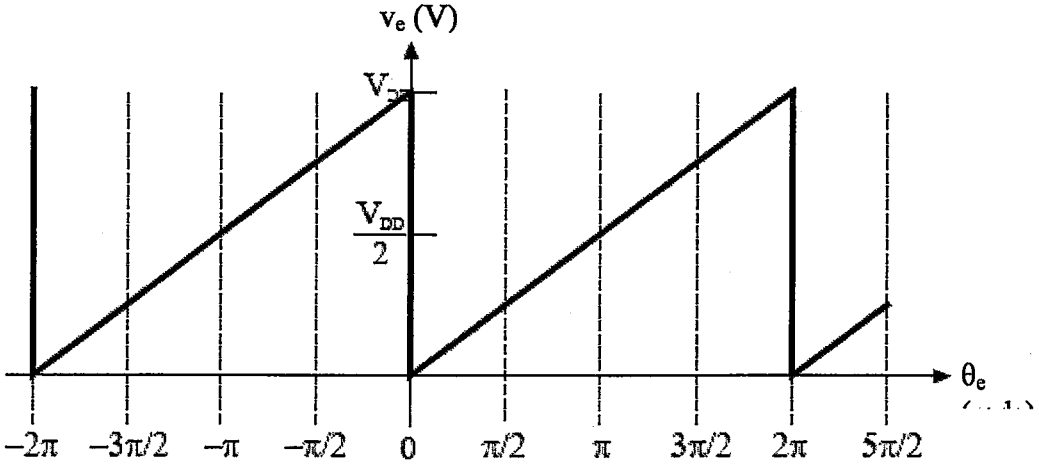


Figure 2.6 SR flip-flop phase detector characteristic.

It is mostly necessary to obtain lock with 0° phase difference. In such cases, an inverter may be added to one of the inputs of the SR phase detector to cancel nominally the 180° phase difference. However, the inverter delay now adds directly to the phase difference, and this is a serious problem particularly at high frequencies. As a result, SR flip-flop is not a suitable phase detector, if 0° phase error is necessary. Furthermore, it is often desirable to extend the phase detection range to span more than one period, 2π rads.

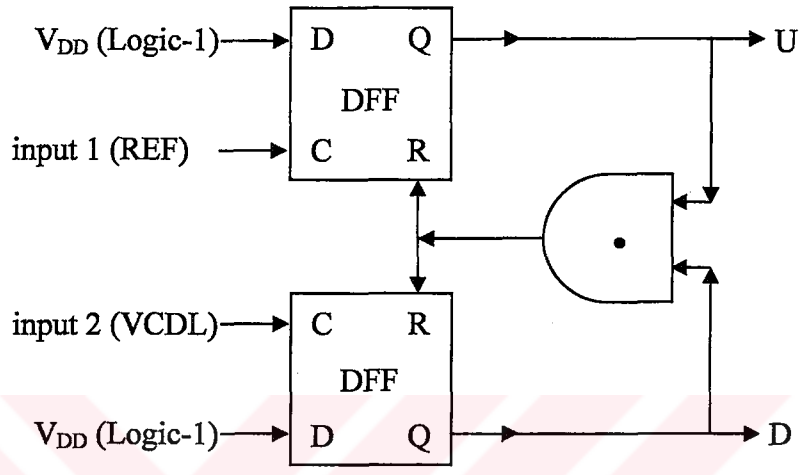


Figure 2.7 Phase/frequency detector.

A more widely used type of sequential phase-detector is the phase/frequency detector (PFD) of Figure 2.7. It is constructed from a pair of D-type flip-flops and an AND gate. Data inputs (D) of the flip-flops are connected to logic-1 and the inputs are applied to the clock inputs of the flip-flops. The output of the flip-flop to which reference signal is applied is U which stands for "up". And the output of the flip-flop to which VCDL output signal had been applied is D which stands for "down". Up and down signals are inputs to an AND gate which drives the reset inputs of the flip-flops. Operation of the phase/frequency detector is illustrated in Figure 2.8.

Assuming that the input signal frequencies are equal and reference input leads VCDL output by an amount θ_e, then after each rising edge of the reference, the U output is set to logic-1. When the rising edge of the VCDL output is received, for an instant both U and D outputs are set to logic-1. This produces a pulse at the AND gate output, the reset inputs, and then U and D outputs are set to logic-0. Ideally, we assume that the AND gate has zero response time. Thus, if the reference input leads the VCDL output, the mean value of the U output indicates the amount of phase lead, while the mean value of the D is virtually zero. Conversely, if the reference lags the VCDL output then the D output becomes active and indicates the amount of

the phase lag. Ideally none of the outputs, U and D, can be active at the same time. The difference of the mean values of U and D gives the phase/frequency detector characteristic.

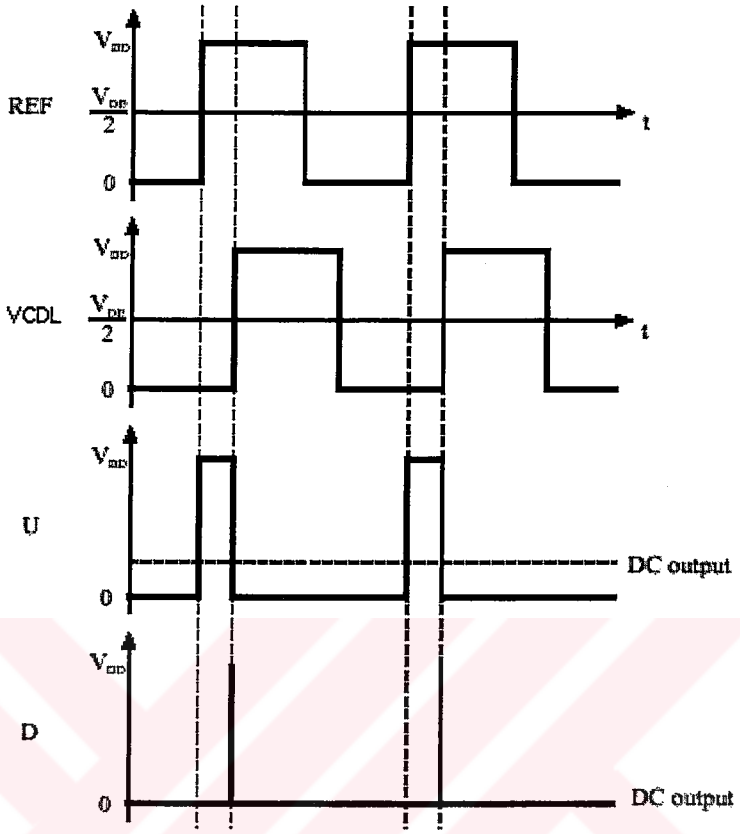


Figure 2.8 PFD operation.

The output characteristic is given in Figure 2.9. It is a sawtooth characteristic with a linear range of $\pm 2\pi$ (4π) rads. So, the phase/frequency detector spans two periods. The phase/frequency detector gain is:

$$K_{PD}=V_{DD}/2\pi \qquad (2.6)$$

which is the same as for the SR flip-flop. It is clear from the characteristic that to maximize the capture range, static phase error should be 0°. Also the DC output is zero for the lock point, which means that there is no need for DC offset compensation in the loop filter.

Time difference of up and down signals corresponds to the phase error of the two inputs. Theoretically the up and down signals zero in locked condition, therefore the output contain no spurious signals at all. In order to achieve this difference value an ordinary differential amplifier could be accommodated. While keeping in mind that these up and down pulses are at the same frequency of the input signal, the differential amplifier needs not to respond these pulses at high frequency but has to respond to the DC component. Usually a special form of

loop filter could be used to achieve these functions of both a differential amplifier and a loop filter, called charge pump, which will be explained in next section.

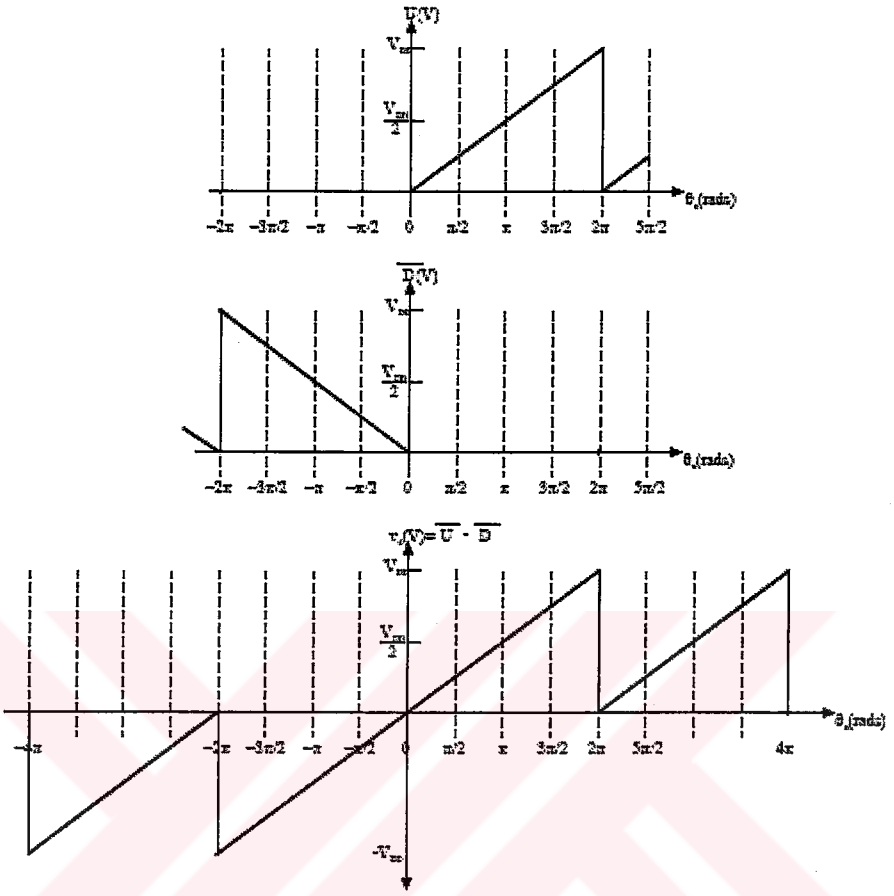


Figure 2.9 Phase/frequency detector characteristic.

There also exist different kind of sequential phase detectors like Bang-Bang (Hogge) phase detector, Alexander phase detector etc, used mostly in clock/data recovery applications with different characteristics [Razavi, B., 2002]. There also exist modified versions of phase detectors like "Precharged phase detectors" and many works have focused on phase detectors for different applications in recent years [Johansson, H., 1998]. But in this work, in order to distinguish leading or lagging output over two periods of reference input, phase/frequency detectors is of interest, which could distinguish not only the absolute phase difference, but also the phase relationship. From this point of view, PFD topology is selected as a phase detector and their partners charge pumps are of interest.

2.2 Charge Pumps

The charge pump could be understood by basic implementation consists of two switched current sources driving a capacitor (Figure 2.10a) [Gardner, F., 1980]. For a pulse width of Δt

on U, I_1 deposits a charge equal to $I.\Delta t$ on C_p. Or for a pulse width of Δt on D, I_2 removes a charge equal to $I.\Delta t$ on C_p. Thus, if the reference signal leads the VCDL output, then positive charge accumulates on C_p steadily, yielding an infinite gain for the PFD.

Thus, the charge-pump introduces a pole at zero to the system. This is why; the charge-pump not only behaves as a differential amplifier but also as an integrating loop-filter. If pulses appear on D, I_2 removes charge from C_p on every phase comparison, driving V_{out} toward $-\infty$. When U and D are both inactive, there is no net change on the charge; V_{out} remains constant (Figure 2.10b). The example is shown for PLL case here in order to be able to show the case for when reference and the output is at different frequencies.

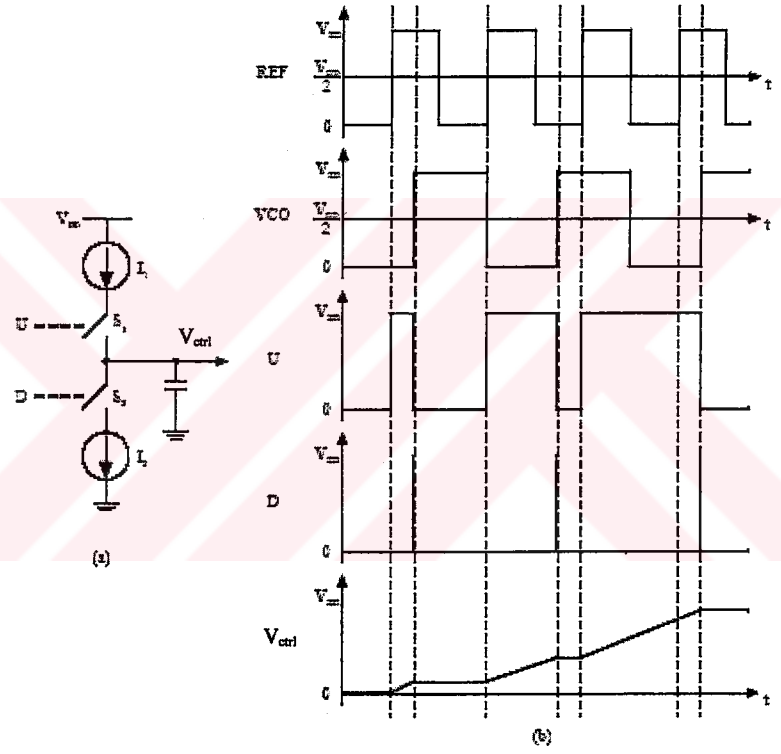


Figure 2.10 (a) Charge Pump and (b) its operation

If the input signals have a phase error of θ_e rads, then the average current charging the capacitor is given by:

$$I_{av}=I_{cp}.\theta_e/2\pi \tag{2.7}$$

and the average change in the control voltage is;

$$V_{ctrl}(s)= (I_{cp}.\theta_e/2\pi).(1/sC_p) \tag{2.8}$$

which can be written in general form of;

$$V_{ctrl}(s)= K_{PD}.\theta_e.F(s) \quad (2.9)$$

Thus, if we combine phase/frequency detector and charge pump, overall gain would be;

$$K_{PD\_CP}=I_{cp}/2\pi \quad (2.10)$$

and the loop filter transfer function is simply;

$$F(s)=1/sC_p \quad (2.11)$$

which is a perfect integrator's transfer function.

The most important problem of the PFD is the crossover distortion, changes in gain that occur near zero phase error. Assuming that the D-type flip-flop outputs exhibit relatively long transition times compared to the AND gate delay (reset-path delay), the reset is immediately activated when U and D exceed the threshold of the AND gate. The goal is to examine the increment in the charge deposited on C_p for an increment Δt in the delay between the input signals or simply the small-signal gain.

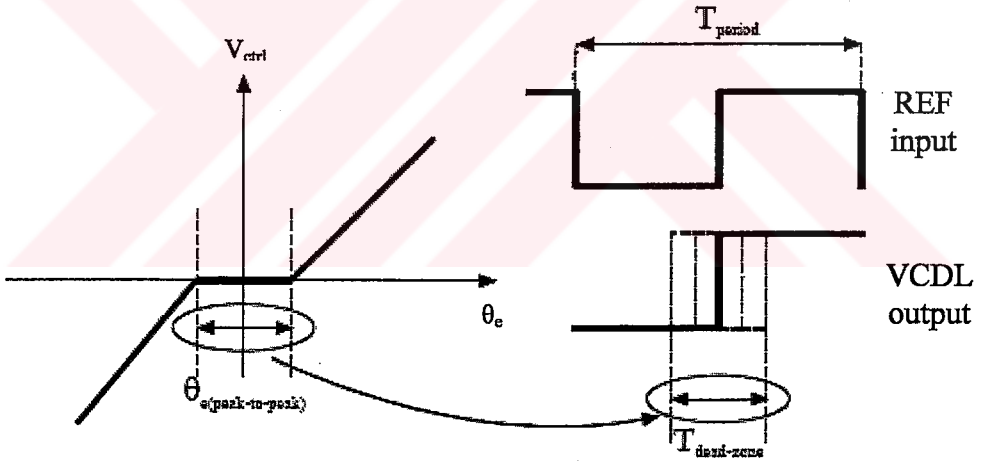


Figure 2.11 PFD dead-zone and corresponding DLL output peak-to-peak jitter.

The phase detector characteristic has a flat response near zero phase difference. This is called "dead-zone". The dead-zone is undesirable in a DLL because the loop is effectively opened (since K_{PD} is zero) and the output spectrum changes accordingly. If the phase difference varies within the dead-zone, the DC output of the charge-pump does not change significantly and the loop fails to correct this error. Consequently, a peak-to-peak jitter approximately equal to the width of the dead-zone arises in the output. Figure 2.11 shows the relation between dead-zone of PFD and the phase error of the DLL. If the phase difference of the reference clock and the VCDL output is smaller than the dead-zone, the PFD cannot detect

the phase difference. The minimum peak-to-peak phase error caused by this dead-zone could be written as;

$$\theta_{e(pp)}=2\pi.T_{dead\text{-}zone}/T_{period} \quad (2.12)$$

To solve this phenomenon, it is obvious that the reset-path delay must be more than the flip-flops' transition delay. When the D output crosses the threshold, the reset signal is not asserted as a result of the extra delay. So, both outputs, U and D, continue rising and reach full logic level if reset-path has sufficient delay. They both stay at logic-1 for sometime and then return to logic-0 when the reset signal arrives. Thus, U stays at logic-1 more than D with a time equal to the phase difference. When both outputs are high, both switches are on and the net charge delivered to the output is zero. So, the net charge is completely defined by the phase difference between the inputs. Thus, the dead-zone disappears only if U and D outputs are simultaneously high for a sufficient amount of time. In lock, both U and D are simultaneously high for a time equal to the reset-path delay.

Another problem about charge pumps could arise from mismatches of current sources I_1 and I_2 and switches S_1 and S_2 in Figure 2.10a. Even if the phase difference is zero, control voltage will vary every comparison period because of mismatched current sources will deposit or remove charges from loop filter capacitance with an amount of I_1-I_2 (assuming $I_1 \gg I_2$). This mismatch current will deposit charges to filter capacitance during reset-path delay time. So it is possible to write down control voltage ripple as;

$$\Delta V_{ctrl}=(I_1-I_2).t_r/C_p \quad (2.13)$$

where t_r is reset-path delay. The current mismatch would cause reference sideband in the spectrum and the value of ΔV_{ctrl} would directly determine the sideband levels.

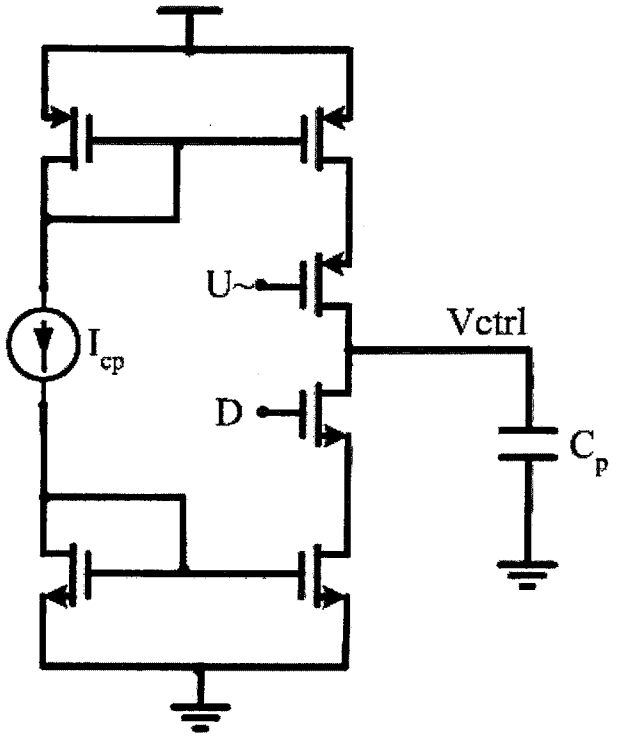


Figure 2.12 Charge pump and loop filter implementation example.

Some practical charge pump implementation (Figure 2.12) problems could arise, for example if the current sources would be designed as MOS current mirrors (PMOS through the V_{DD} and NMOS through the ground), besides mismatches, current sources could not be able to supply desired current values if the control voltage reaches one of the supply rails. So enough voltage headroom has to be supplied to the current sources. These levels would be boundary for control voltage, so achievable amount of delay should be examined at these control voltage levels of VCDL. If the current sources leaves saturation and enough voltage headroom could not be supplied, this would degrade the gain of the block that would directly affect DLL, so that DLL loop dynamics should be carefully investigated under these circumstances.

If S_1 and S_2 switches were implemented as MOS switches and they were off, a recovery time necessary to go on. If this time longer than the phase difference, dead-zone phenomenon would appear. Also, when the switches are at off state charge injection and feedthrough mismatches would cause the control voltage to be disturbed. Parasitic capacitances also should be taken into account; those who are parallel to the loop filter capacitance would affect the calculated DLL bandwidth. Charge sharing mechanism around the filter capacitance and the other parasitic capacitances (for example; drains of current sources) would make control voltage to jump some value, which could cause reference sidebands at the output of the DLL.

Different kinds of implementation approach could be useful in order to solve current mismatching, device parasitic effects, fully turning on and off effects of the devices and others. For example, a differential charge pump could increase noise immunity. Also accommodating only one current source would completely remove current mismatch's unwanted effect to the DLL like spurious tones at the output.

2.3 Loop Filters

Loop filters would directly affect the bandwidth of the DLL as will be explained in chapter 4. In contrast to PLL, DLLs are inherently stable so there is no need neither lag nor lead-lag nor different kind of filters, only a pole at zero is enough. This first order filter is only a capacitor at the output of the charge pump, as could be seen in Figure 2.12.

In special cases like jitter amplification phenomenon and some modified versions of DLL like re-circulating DLLs, second or more ordered filters could be necessary. But these are of concern at this time.

2.4 Voltage Controlled Delay Line

Voltage controlled delay line (VCDL) is the most important part of the DLL because its performance dominates DLLs features such as capture range, inherent noise behaviors, spectral purity. Thus VCDLs could have the following characteristics in order to achieve a properly working DLL having advantageous noise behavior;

VCDL should have monotonic transfer function within the tuning range: VCDL's gain could be thought as the ratio of the output phase/delay and control voltage. Monotonicity means that only one delay value corresponds to a control voltage. This feature prevents DLL to lock to an incorrect state or to latch-up.

Figure 2.13 shows two possible transfer functions for DLL. If the VCDL having a transfer function like parabolic curve in the Figure 2.13a, it is possible that the loop could not be able to lock the output phase to the reference. This could be understood by considering a phase difference $\Delta\theta$ between the reference and the output at the initial state. Phase/frequency detector would compute the absolute of phase difference and its direction (whether the output leading or lagging the reference) and the charge pump would produce a control voltage using phase/frequency detector output. So the feedback loop would increase or decrease the control voltage to add more delay (or decrease the delay) in order to approach the output to the

reference. But the transfer function like parabolic curve, loop could not be able to distinguish the demand on control voltage acts whether increase or decrease. So it is likely that VCDL total delay would stack to one of the extreme cases, meaning false locking to a state with a static phase error.

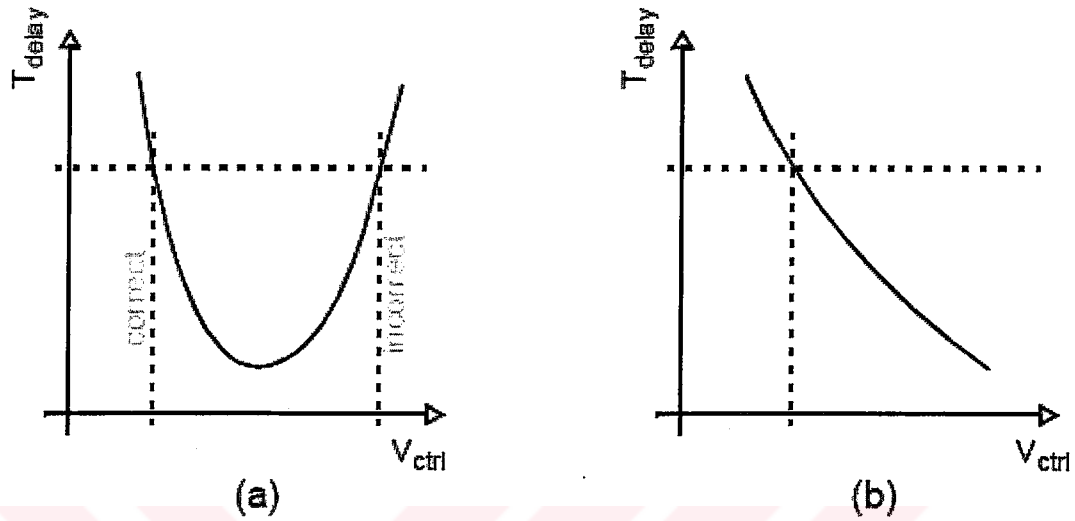


Figure 2.13 Some possible transfer functions for DLL

With the aid of transfer function seen in the Figure 2.13b, loop would determine direction whether increasing or decreasing the control voltage (so the VCDL's total delay) in order to achieve zero phase difference between output and the reference. Monotonic transfer function would avoid DLL to lock an incorrect state within the tuning range.

VCDL should have a controllable amount of delay at least equal to the reference period: Although the phase/frequency detector used in this implementation determines the phase offset between input and output, it does not always match corresponding edges from the correct input and output pair. For instance, in Case 1 of Figure 2.14, if output is severely leading input by more than $T_{ref}/2$, the phase/frequency detector may determine that output is lagging the previous edge of input by less than $T_{ref}/2$ and try to adjust the control voltage to speed up the VCDL even further. The opposite can also happen when output is severely lagging input by more than $T_{ref}/2$, shown in Figure 2.14, Case 2. Therefore, to avoid the above situation, signals presented at the phase detector inputs need to be within a certain range, ideally within $\pm T_{ref}/2$, to guarantee correct phase detection.

The total phase delay of the VCDL needs to be within $\pm\pi$ of the reference period by design including PVT (process, voltage, temperature) variations. In general, VCDLs are designed to have controllable delay more than one period of the reference and even equal to two periods

of the reference. But under this circumstance this feature should be handled carefully by start-up conditions of the loop and control logic, determining which edge to be locked.

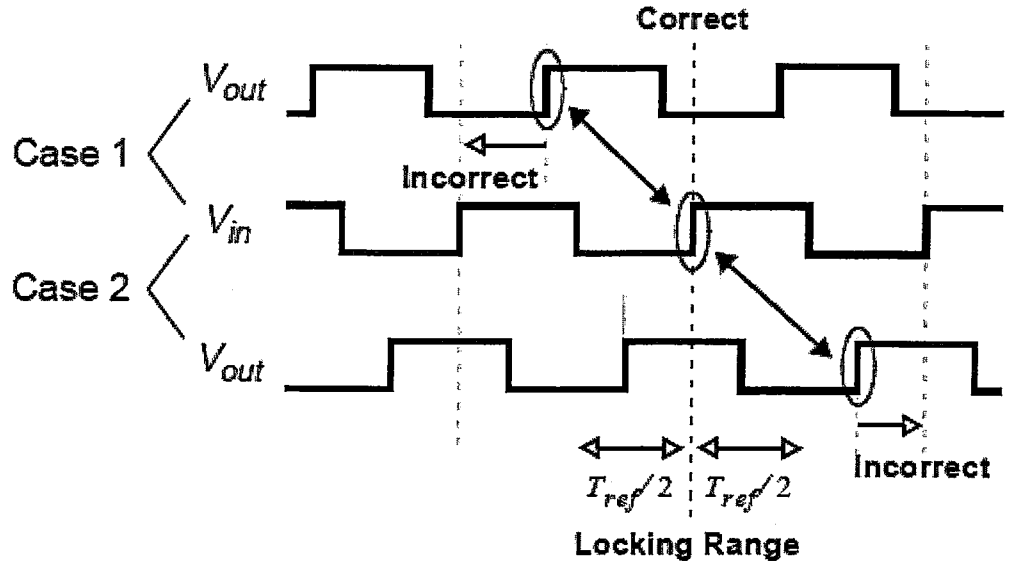


Figure 2.14 Phase difference detection range

Delay stages forming VCDL should be identical: Firstly, this feature is not valid for passive implementation of VCDL, for example transmission line with tunable phase shift along the delay line and also for active implementations for DLL used in skew cancellation applications. Because feedback loop compares only the output of the VCDL, not any of inner nodes, with reference and locking occurs for the output phase. But application areas of multiphase clocking and frequency synthesizing, inner nodes of VCDL containing different phase shifted versions of the reference, carry useful information. These applications rely on the equally divided phase shifts of reference period. In order to exploit DLLs different application areas, each delay cell need to have identical phase/time delay and to be adjusted uniformly.

This feature lowers the levels of spurious tones at the output of the frequency synthesizer or interleaved processing units. Also using identical delay stages brings design simplicity for the VCDL.

2.4.1 Delay Stages

Voltage controlled delay lines could be constructed from basic delay elements called "delay stages (=delay cells)". Simply, a delay stage adds some constant delay and a controllable delay to its ingoing signal. It is not always possible to achieve desired controllable amount of

delay with one stage. In order to achieve enough adjustable delay and characteristics listed above, VCDL could be formed from number of delay stages. Also, multiphase clocking requirements or frequency multiplication factors could dictate the number of delay stages in the VCDL.

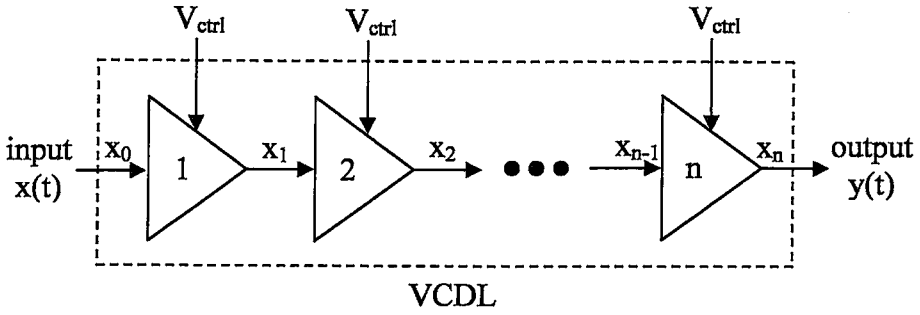


Figure 2.15 Voltage controlled delay line block diagram.

Figure 2.15 shows VCDL block diagram built up "n" delay stages. Each stage could be thought as buffer stages with control input. VCDL could be designed as to have a delay of multiple of reference frequency period, $m \times T_{ref}$. In locked condition, output and input of the VCDL would be in-phase. If m=1, each buffer output would be evenly spaced in reference frequency period, $x_{1,2...n}$. so T_{ref}/n spaced multiphase clock signal were available for interleaved processing. And also these signals could be used in frequency multiplication and multiplication factor would be equal to number of delay stages, n. Value of m could also be more than one, and so VCDL could output multiple of reference frequency period divided by number of delay stages, n. In general, frequency multiplication factor or multiphase clocking factor would be;

$$F=T_{ref}.m/n \tag{2.13}$$

If "m" is greater than one, DLL dynamics should be carefully investigated in discrete time domain, because stability problems could occur. Defining number of delay stages, n, relies on implementation issues and application area of DLL.

As mentioned before, VCDL could be constructed with passive devices and transmission lines. These methods could prevent multiphase clocking and frequency multiplication features of the DLL if only one stage operating as VCDL. In Figure 2.16 a simple implementation example had been shown. An on-chip inductor and a capacitor could be used to form a resonator. Varactors could be implemented as variable capacitor to tune the phase shift of the stages. Numbers of resonant stages could be used in VCDL in order to get the advantage of

multiphase reference signal. Passive VCDL would result better noise performance with respect to active devices. On-chip inductors occupy large silicon area and low quality factors (Q) and very low matching properties make this solution unfeasible.

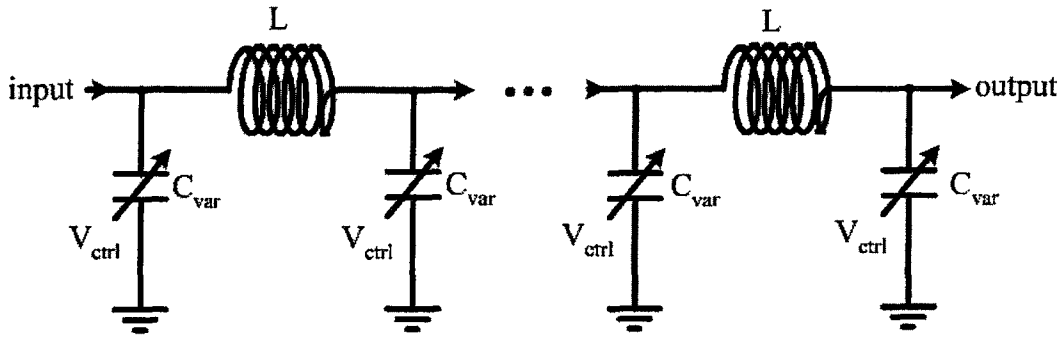


Figure 2.16 Passive implementation of VCDL.

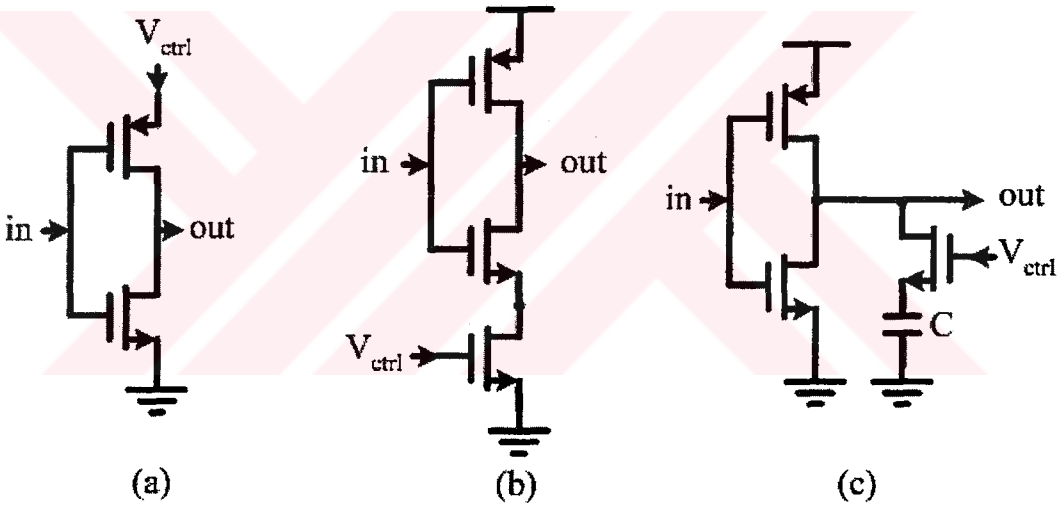


Figure 2.17 Implementation examples of single-ended delay stages.

Active buffer stages and inverters are widely used in DLL applications as delay stages. In Figure 2.17 some CMOS implementation examples had been shown. Each of the circuits has different delay setting mechanisms. First, adjusting positive supply would speed up or down the inverter stage. Second, adjusting tail current would again control the delay of the inverter and third, adjusting the capacitive loading of the inverter and so delay of the stage (note that capacitor C, could be implemented as NMOS capacitor connecting source and drain terminals to the ground and adjusting the AC capacitance seen from the gate terminal). These circuits are widely used in megahertz range DLLs occupied in digital circuits. But as the operating frequencies increase their supply noise sensitivity and speed limitation of CMOS devices

make them useless (in deep sub-micron processes speed limitation could be overcame). Interstage gain considerations are also important in these implementations, changing voltage gain of the stages, affects rise/fall times of the signal resulting jitter.

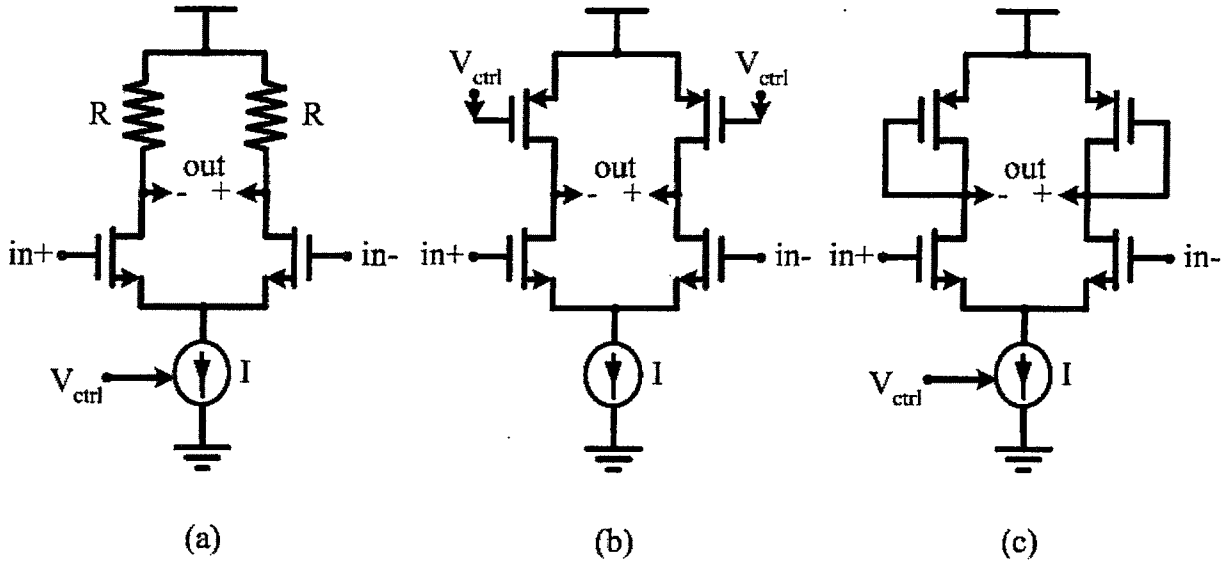


Figure 2.18 Implementation examples of differential delay stages.

Differential delay stage implementations could be useful at high frequencies, with higher noise immunities and lower voltage swings. As could be seen in Figure 2.18a delay control could be done by changing the tail current of the buffer stage. Tail current would affect the switching speed of the NMOS devices, but changing tail current will output voltage swing, I×R, could affect the driving capability of next identical stage and resulting different amount of delay between preceding and following delay stages, which is an undesired result. If the voltage gain of the stages becomes lower and lower, the ingoing signal would not be able to reach to the VCDL output. High quality resistors are also not available on digital CMOS technologies, which necessitate using complicated fabrication steps offering on-chip passive elements, such as RF capable processes. But higher speeds achievable because of resistor. Second example seen on Figure 2.18b delay adjustment could be done by means of changing the on-resistance value of active PMOS triode loads. Changing the resistance would change the time constant of the output node, $\tau=R_{eff,out}\times C_{eff,out}$, by the same amount, yielding a change in the delay of the stage. This stage's output swing also varies with the control voltage, which could be problematic as mentioned before. In Figure 2.18c diode connected PMOS loads and variable tail current source have been used. Adjusting tail current would vary the loads accordingly and the voltage gain would remain constant. But large signal output swing would be depending on tail current. The problems explained above, more or less could be seen in

this topology. There are also some circuits had been developed to overcome some of the above problems like controlling both the load and tail current in a feedback system in order to keep the voltage swing constant, called "replica bias feedback" by Maneatis. This approach could result better jitter performance but it is obvious that this feedback system's bandwidth would have to be large enough with respect to the DLL bandwidth in order to do its tasks properly, explained in [Maneatis, J., 1996].

As a result, delay adjustment of a buffer could be done in two ways; manipulating the switching speed of the active devices by controlling the biasing conditions of the transistors or controlling the time constant of the output node of the buffer either by adjusting the capacitive or the resistive component.

2.4.2 VCDL Transfer Function

In order to determine transfer function of the VCDL, first of all delay stages could be considered in input/output characteristics point of view. In active buffer implementation of VCDL, each delay cell will contribute a minimum delay that is dependent on technology or chosen circuit topology speed limitations. Thus, delay of the each stage constructing VCDL could be decomposed into two terms;

$$T_{dps}=\tau_{dps}+\Delta\tau_{dps} \tag{2.14}$$

first term represents the minimum delay of the delay cell and the second term is the variable portion of the total delay of each cell (subscript "ps" is the abbreviation for "per stage"). Using the definition of delay per stage, total delay of n-stage VCDL could be written as;

$$T_d=\left[\sum_{i=1}^{n}T_{dps,i}\right]=\sum_{i=1}^{n}\tau_{dps,i}+\sum_{i=1}^{n}\Delta\tau_{dps,i} \tag{2.15}$$

equation (2.15) determines two important parameters of the VCDL. First term, the sum of the minimum delay (or constant delay), would state that the number of cycles of the reference frequency period to be locked at and the second term would determine the lock range of the VCDL. First term would help calculating the "m" value seen in the equation (2.13). In locked stage VCDL should have total delay of multiple of the reference frequency period (m=1,2,..). Second term has to be larger than the reference frequency period at all PVT variation conditions, which is the lock range of the DLL.

VCDL's characteristic could be written in phase domain rather than time domain, that is;

$$\theta_d = \frac{2\pi}{T_{ref}}\left[\sum_{i=1}^{n}\tau_{dps,i} + \sum_{i=1}^{n}\Delta\tau_{dps,i}\right] \tag{2.16}$$

where T_{ref} is the period of reference frequency.

VCDL transfer function is input-output phase difference versus control signal, resulting with the unit of radian/volts.

$$F_{VCDL}(s) = K_{VCDL} = \frac{\theta_d}{\Delta V_{ctrl}} \tag{2.17}$$

where ΔV_{ctrl} is the control voltage operating range. This equation could also accommodate "$-m.2\pi$" depending on the definition of the transfer function. It should be noted that, first term of the θ_d in equation (2.16) is constant, and second term will vary with the control signal. This feature should be taken into account while investigating the loop dynamics of the DLL. Especially if the first term is more than couple of times of the T_{ref}, stability of the DLL could be affected. It is also worthy to keep in mind that, loop would not be able lock the VCDL output, lower than multiple of the reference period dictated by this value.

Main difference between the DLLs and PLLs arise from the equation (2.17); VCDLs have a constant gain, K_{VCDL}, while VCOs transfer function is in integration form, K_{VCO}/s, introducing a pole at zero (phase is the integral of the frequency).

2.5 DLL Application Areas

After determining the basic principles of DLLs, it would be easier to define the "DLL solution" to some problems of either system level or performance metrics point of view, in modern ICs. DLL application areas will be discussed in detail in following sections.

2.5.1 Skew Cancellation

Skew could be called as unwanted phase shift of a synchronizing signal, such as clock signal. This unwanted phase shift could be harmful on circuits operations, which were clocked with the same signal cause of getting lost of synchronization by means of either system level or circuit level point of view. This phenomenon could occur whether in printed circuit boards, PCBs, or integrated circuits, ICs.

Second reason that causes the skew is the different length of electrical wires on each clock path. If these electrical wires are ideal, there is no skew of course. But it is not the case in reality so electrical wires should be modeled with a parasitic resistor and a capacitor and even

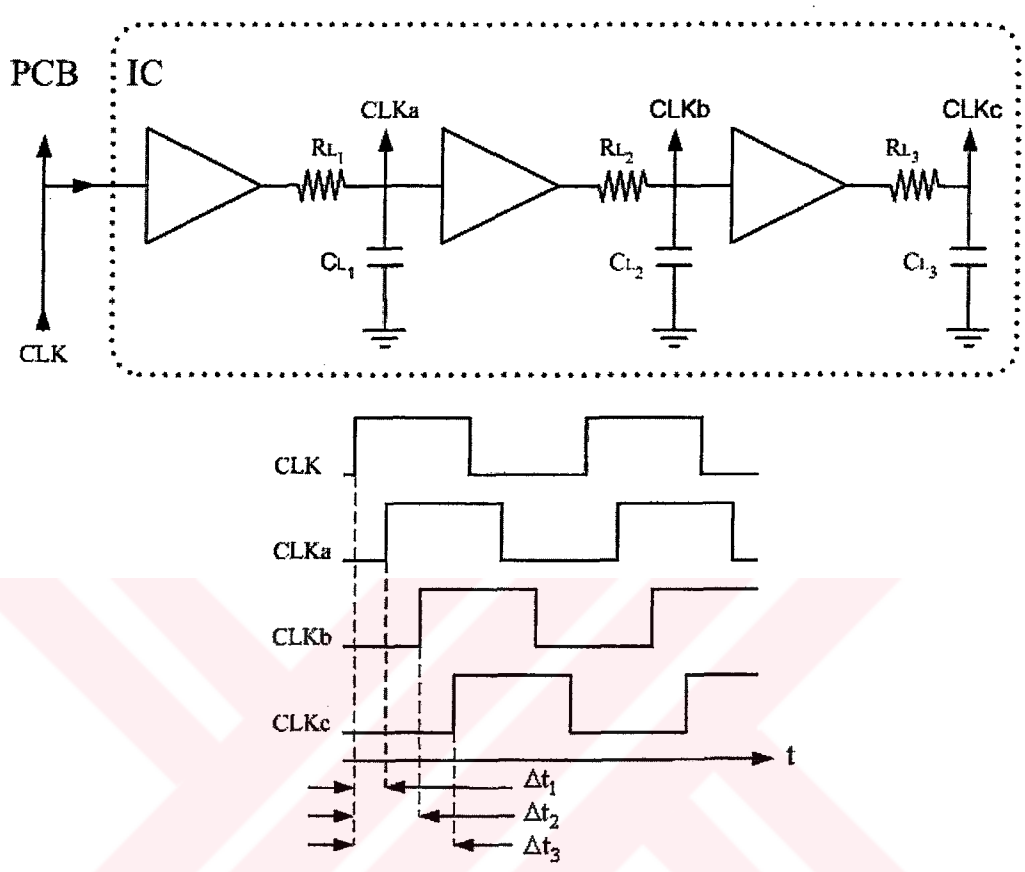


Figure 2.19 Formation of "skew" phenomenon in ICs.

with a parasitic inductor, either lumped or distributed way. If we ignore parasitic inductor for instance at low frequencies, a first order model could be seen in the Figure 2.19. Different time constants, $\tau=R_{L,n}\times C_{L,n}$ (n=1,2,3) at either nodes would result different delay in clock signals as mentioned before even if the buffer stages seen on the figure introduce zero phase shift. Proper layout techniques could reduce the amount of skew at first glance. Same length and width of each clock path wires could result almost same amount of parasitic element values resulting equal time constants at each nodes.

In some cases, skew could not be handled with basic solutions like clock distribution networks, equaling the number of the buffer stages and wire lengths seen in the Figure 2.20. Thermal gradient whole over the IC, would have an effect on the performances' of buffer stages and parasitic element values of the electrical wires. Thus, solutions rely on layout techniques incapable of eliminating skew if the large silicon area and long clock path lengths are the concern, but some reduction is achievable. If the operating frequency increases,

ignoring parasitic inductance could result deadly amount of skew. At higher frequencies, also lumped parasitic model would not be able to model the skew, thus distributed behavior of the parasitic elements reduce the reliability of the layout techniques. Thus, active synchronizers incorporating feedback systems such as DLLs and PLLs have to be called to duty.

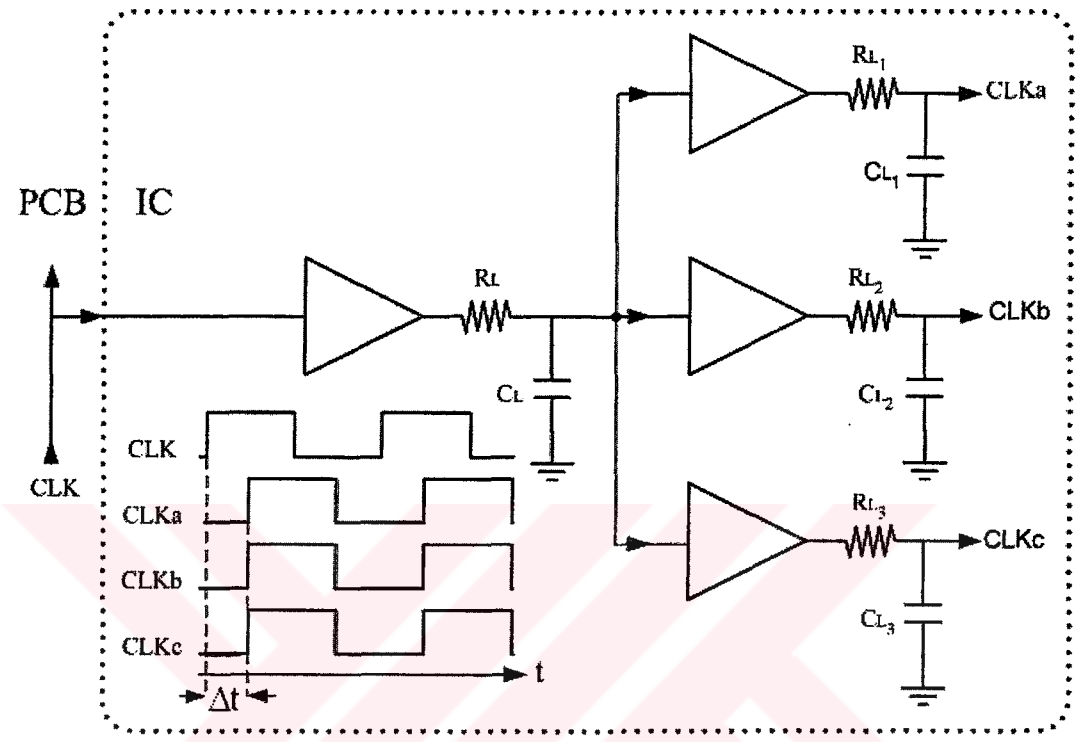


Figure 2.20 Reduction of skew with a clock distribution network.

DLLs and PLLs could be used to eliminate skew problem. Suppose an electronic system, built up with synchronized two sub-blocks or systems with a clock signal, and second block clock input load makes using of a strong clock driver inevitable, in Figure 2.21a. Clock driver could introduce significant amount of delay to the clock signal causing skew between its input and output, CLKa and CLKb, could cause the system malfunction. In order to eliminate the skew caused by the clock driver, a DLL could be incorporated to the system given in Figure 2.21b (Sub-block/System-1 is not shown for clarity). If the clock driver that has significant amount of delay, could be accommodated in the feedback path of the loop. In this case, phase detector would compare CLKa and delayed version of it, CLKb, and produce an error signal in order to correct the phase delay of the VCDL, resulting zero phase difference between CLKa and CLKb in locked condition. Thus, significant delay of the clock driver should be eliminated, leaving system to work properly, in terms of synchronization.

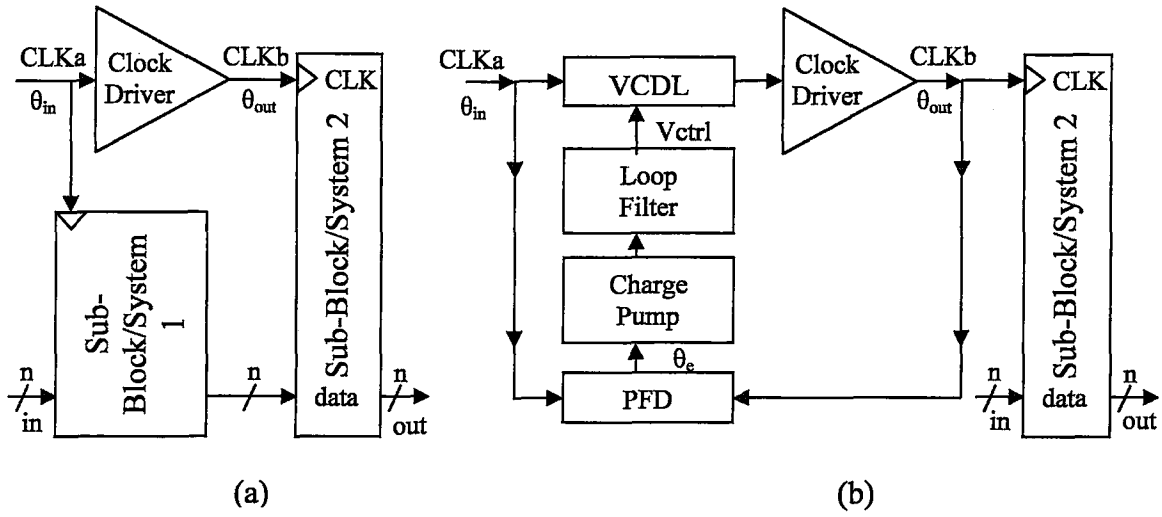


Figure 2.21 DLL used in skew cancellation application.

It should be noted that electrical wires are assumed to be ideal in above explanation but it is not the case. If the wire lengths introduce an amount of delay at feedback path because of the parasitics of the wire, DLL would lock to a nonzero phase shift, which is equal to the phase difference of the two paths of phase detector inputs. This situation should be examined by means of the synchronized blocks of the system, whether causing a problem or not. If the driver delay is at the order of a couple of clock signal period, T_{ref}, DLL dynamics should be investigated. This extra delay could be problematic by means of stability so careful modeling of this situation is vital.

High frequency synchronization applications could be more problematic by means of skew cancellation. Considering 1GHz (T_{period}=1ns) clock signal narrows the timing budget of synchronization even in cascading stages, keeping in mind that minimum gate delay of sub-micron CMOS technologies is at the range of a couple of hundred picoseconds. As the clock frequency increases further, say it 4 GHz, time budged lower to 250ps. Consider a Flash ADC with a track-and-hold (T&H) amplifier used in its input and data rate at 4Giga sample per second as shown in Figure 2.22. T&H amplifier tracks its analog input one half period of the clock signal, 125ps for 4GHz clock, and holds the value during the other half period of the clock, 125ps (Instead of T&H, sample-and-hold circuit (S&H) could be used. S&H could be considered as two cascaded T&Hs working on 180° phase shift. But at high frequencies, ideal sampling could not be accomplished thus, mostly one T&H stage takes place at the input of the Flash ADC). During hold period, comparators will decide the level of the constant input value and produce corresponding digital word in thermometer code. Then digital encoder will convert the digital word to the binary code. These blocks should be worked in synchronized.

Clock skew would be problematic in these kind of over gigahertz range applications, because of very low timing budget, 125ps in above example. If these blocks could not be able to work synchronized, comparators would have decide according to an improper input value, such as tracking phase output of the T&H stage or a transition region output. This inappropriate decision time could worsen static and dynamic behaviors for ADCs, such as SNDR (signal-to-noise plus distortion ratio) and SFDR (spurious free dynamic range) and ENOB (effective number of bits). It is not convenient to feel confident reducing skew only with layout techniques but active synchronizers should be take place.

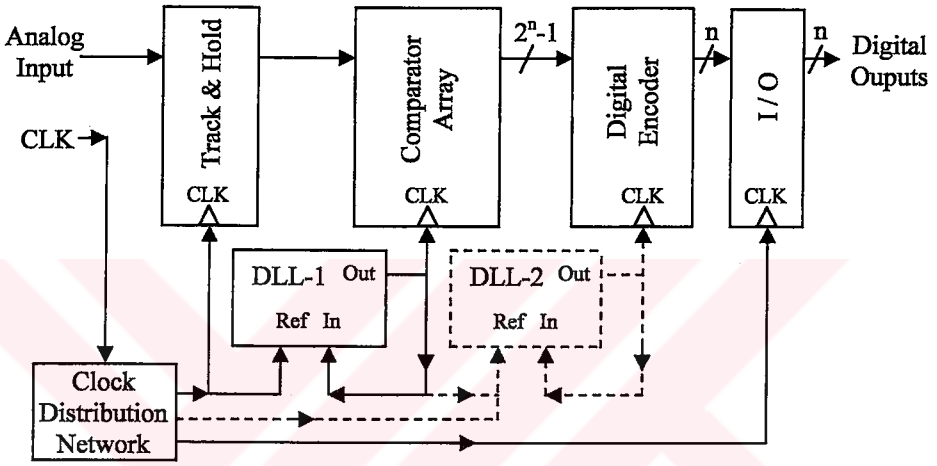


Figure 2.22 Very high sample rate Flash ADC block diagram with skew cancellation DLLs.

DLL-1 in the block diagram reduces the skew between T&H and Comparator Array, allowing proper operation of cascading blocks even with very low synchronization timing budget. A second DLL could be used to synchronize comparators and encoder stages. Reference point for DLL-2 either could be first node of the clock signal, which corresponds to T&H's clock signal or preceding stage, comparators' clock.

A noise property of clock signal, in terms of peak-to-peak jitter, directly affects the ADC dynamic characteristic. It is well known that signal-to-noise ratio of an ADC resulting from the quantization noise is [Razavi, B., 1995];

$$SNR(dB) = 6.02N + 1.76 \tag{2.18}$$

and ENOB could be written as;

$$ENOB = \frac{SNR(dB) - 1.76}{6.02} \tag{2.19}$$

SNR value caused by the clock jitter;

$$SNR(dB) = -20\log(2\pi f_o t_{jitter(rms)}) \tag{2.20}$$

considering overall system performance, SNR becomes;

$$SNR(dB) = -20\log\left((2\pi f_o t_{jitter(rms)})^2 + \left(\frac{1+\varepsilon}{2^N}\right)^2 + \left(\frac{V_{noise(rms)}}{2^N}\right)^2 \right)^{1/2} \tag{2.21}$$

where f_o is the frequency, ε is the average DNL of the ADC, $t_{jitter(rms)}$ is the root-mean-square jitter of the clock signal, $V_{noise(rms)}$ is the thermal noise in terms of LSB (least significant bit) and N is the number of bit of ADC. Equations (2.19) and (2.21) directly determines the dynamic behavior of ADC so as could be seen in from the (2.21) larger clock jitter could reduce the SNR value of the ADC, which is an unwanted situation. Thus, active synchronizer used in ADC as clock skew canceller, shown in Figure 2.22, should provide better noise behavior.

According to these formulations, for a given rms clock jitter, achievable ADC resolution in effective number of bits versus sample rate graph is obtainable (Figure 2.23). it could be seen that for 4GHz clock signal, 4ps rms jitter results 4 effective number bits. In order to achieve ENOB=8 at the sampling rate of 4 giga sample per second, 4GHz clock signal should have lees than 0.25ps rms jitter which is very hard to accomplish. PLLs could be used in place of DLLs as mentioned before, but these rms jitter values are not obtainable with conventional ring oscillator PLLs. Excellent jitter performance of DLLs over PLLs make them attractive at very high speed applications like ADCs but it should be noted that, according to above formulations, in order to increase the resolution of ADC one bit, rms jitter of the clock signal has to decrease %50. It is important to keeping in mind that accommodating T&H amplifier in front of the ADC would relax the synchronizer jitter performance, if a low jitter clock source drives the T&H amplifier because this tighten jitter specification is still valid for T&H amplifier. ADC block diagram example incorporating skew canceller DLL shown in Figure 2.2 is the case.

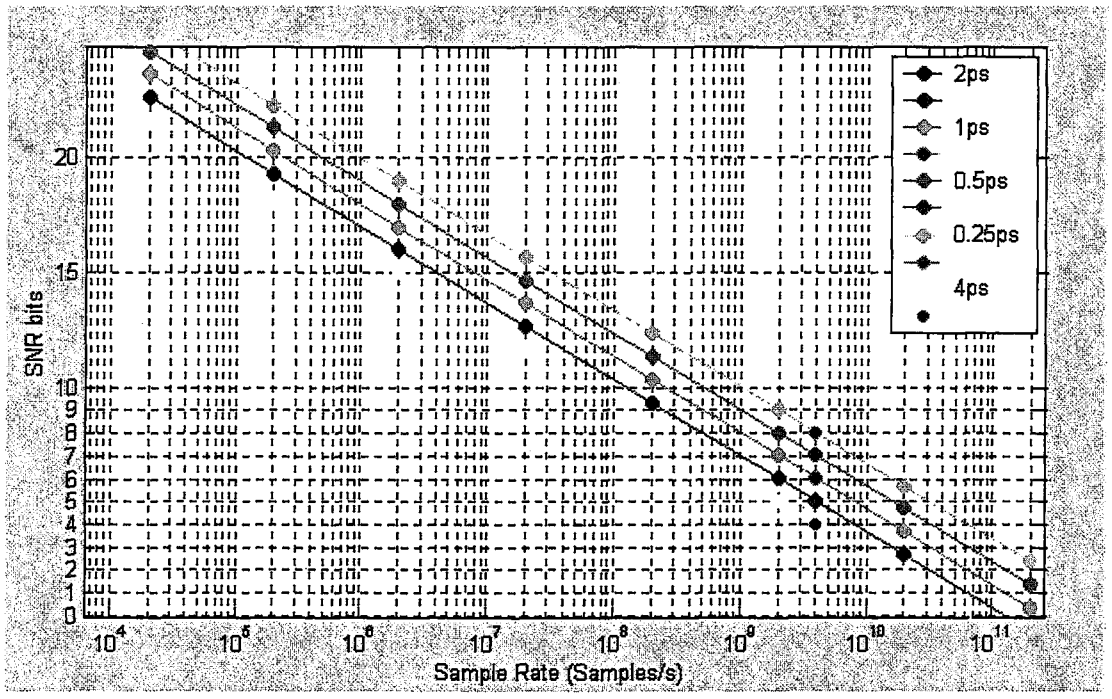


Figure 2.23 Sampling rate versus ENOB for a given clock jitter in ADCs.

It is worthy to give the plot of the equation (2.20) (Figure 2.24). In order to increase the dynamic range of ADC, rms clock jitter should be drastically reduced. Figure 2.25 shows the theoretical limits for achievable resolution for a given sample rate (some of them is defined by the equation (2.21)) [Walden, R.H., 1999], where "aperture" is the clock jitter, "ambiguity" is the sampler delay uncertainty. The upper limit is determined by the Heisenberg's theory as shown in the figure.

Further jitter analyses and DLLs' jitter performance analysis could be found in chapter 3.

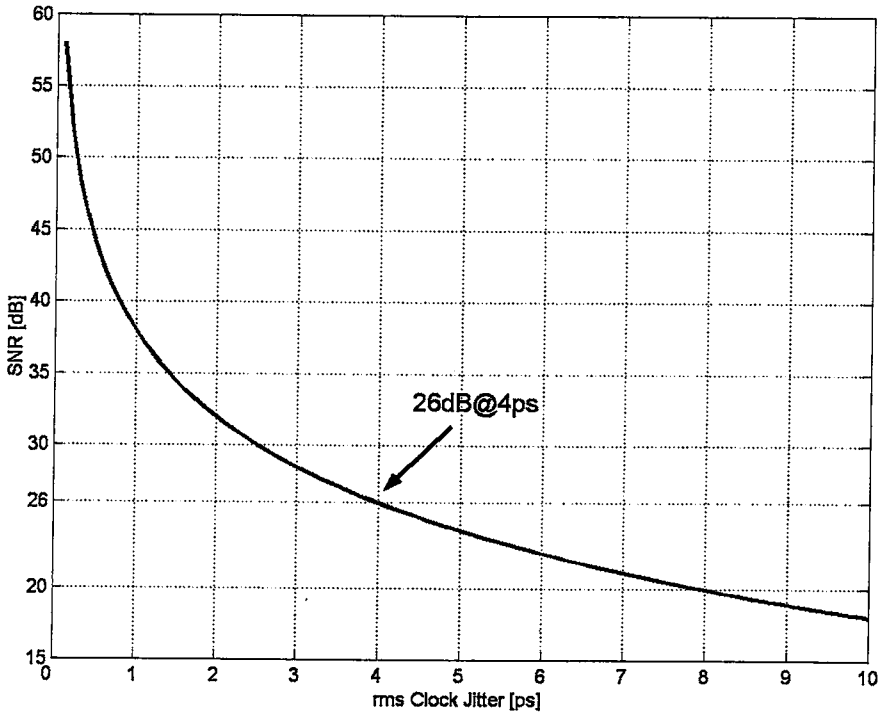


Figure 2.24 Resolution versus rms clock jitter in ADCs.

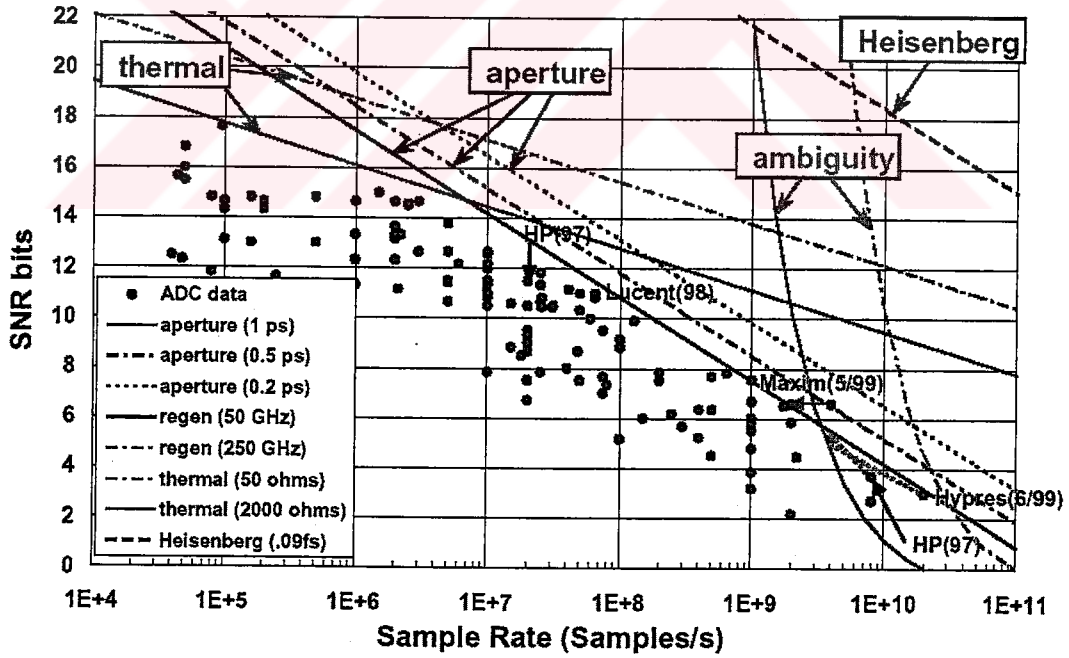


Figure 2.25 Resolution versus sample rate for other system imperfections in ADC

2.5.2 Multiphase Clocking

Increasing demands on achieving higher data processing capabilities make the process technologies lead to the edge. Higher costs of leading edge technologies and possible incapability's of them force the designers to focus on kind of processing techniques like paralleling the processes. This technique takes interest on achieving very high sample rates at ADCs. Usually known as Time Interleaved ADCs' principles rely on this technique.

Consider an over giga sample rate ADC which is very hard to implement with standard CMOS process technologies. It is possible that using "n" unit separate ADCs in parallel, gives an opportunity achieve higher sample rates (Figure 2.26a). First ADC would produce a digital word for its analog input's value at sampling moment. Consider a second ADC working with amount of delay at sampling moment with respect to the first ADC, producing another digital word for its analog input's value at its own sampling moment. "n" stage ADCs could work in same manner. Properly combining the outputs of these ADCs would result a sample rate of n times of a single ADC. The amount of delay on the clock signals of each ADC should be equal with each cascading ADC. Thus, each ADC has to be clocked with evenly spaced phase shifted versions of reference clock signal. If the phase shifts of the clock signals are not equal, some unwanted spurious tones would alias in the Nyquist bandwidth of the ADCs, results worse dynamic characteristics compared to single ideal ADC with a sample rate equal to n times of above ADC.

The deviation of phase delay, or skew, causes severe distortion in the sampled analog signal. It is important to investigate the effect of skew on the dynamic characteristics of ADCs. The noise power P_S caused by the skew is given by [Suzuki, A. and Kawahito, S., 2002].

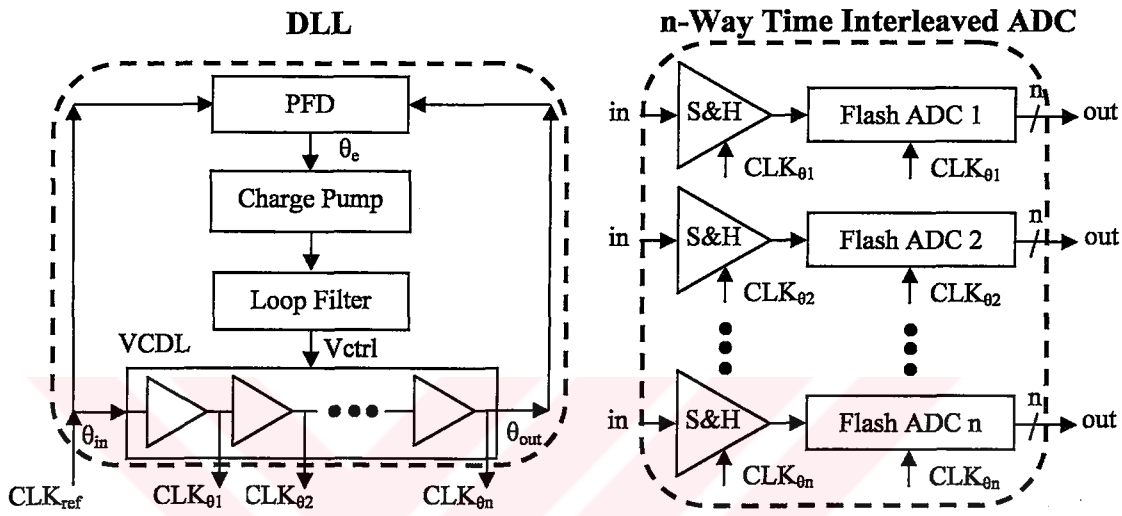
$$Ps = 2\pi f_{in} A^2 \sigma_s^2 \tag{2.22}$$

where σ_s^2 is the variance of skew, f_{in} is the input signal frequency, and A is the input signal amplitude. The total SNDR due to the skew and quantization noise for an N-bit ADC is given by [Suzuki, A. and Kawahito, S., 2002],

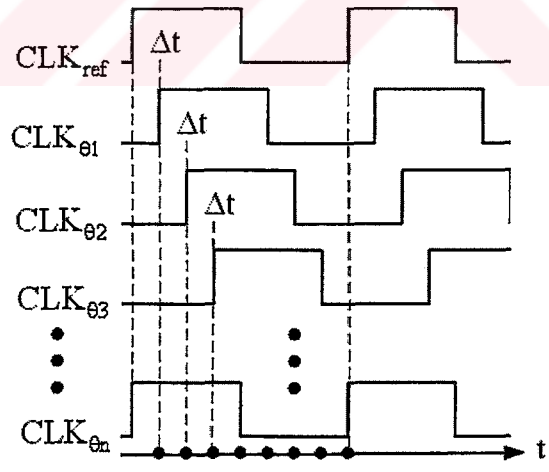
$$SNDR = -10\log\left(4\pi^2 {f_{in}}^2 \sigma_s^2 + \frac{2}{3\times 2^{2N}}\right) \tag{2.23}$$

according the equation (2.23) for example, if the SNDR is required to be more than 70dB in 14b ADC, the standard deviation of skew must be less than 1ps.

The evenly spaced clock signals could be generated by a DLL (Figure 2.26a). DLL would lock its output to its input with zero phase difference, $\theta_e=\theta_{out}-\theta_{in}=0$. At the same time, total VCDL delay would has to be equal to one reference frequency period, $T_{ref}=1/CLK_{ref}$ (as mentioned before, total VCDL delay could be equal to multiples of T_{ref}, depending on the design). If the delay stages used in VCDL were equal, each delay stage output would produce evenly spaced versions of the reference clock signal, $CLK_{\theta 1,2,..,n}$ (Figure 2.26b).



(a)



(b)

Figure 2.26 (a) n-way time interleaved ADC with a DLL generating multiphase of the reference clock signal. (b) multiphase clock signal generated by each delay cell of VCDL.

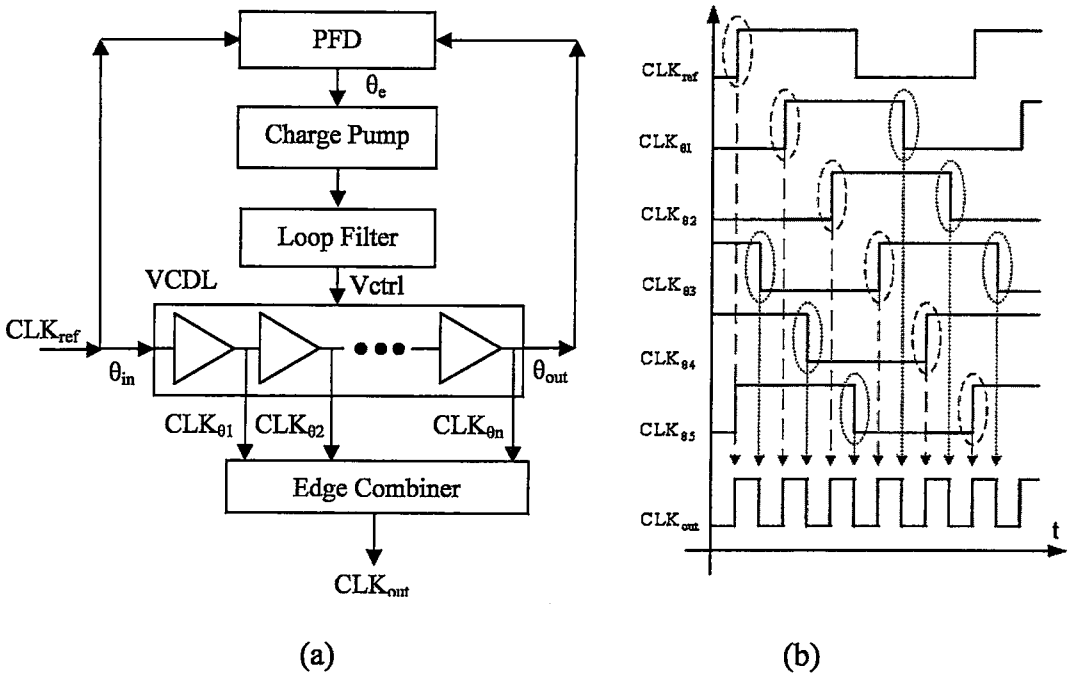


Figure 2.27 (a) DLL-based frequency multiplier and (b) its operation

2.5.3 Frequency Synthesizying

In locked condition, DLL could provide evenly spaced versions of reference signals, if the delays stages built up VCDL are identical, as mentioned before. Evenly spaced clock signals are at the same frequency with the reference clock signal. Multiphase clock signals carry useful information for frequency multiplication (Figure 2.27a). If, somehow, it is possible to combine the each edge of the evenly spaced clock signal, the output signal will be at number of delay stages, n, times the reference frequency. Edge combiner operation for five delay stages example is shown in Figure 2.27b.

In order to find the frequency multiplication factor, in locked condition of the loop delay per stage could be written as;

$$\tau_{dps} = \frac{m \times T_{ref}}{n} \tag{2.24}$$

where τ_{dps} is the delay per stage, n is the number of delay stages T_{ref} is reference frequency period and m is number of cycles of reference frequency period to be locked. In general, as could be seen in the Figure 2.227b, the output frequency is;

$$f_{out} = \frac{1}{\tau_{dps}} = \frac{n}{m \times T_{ref}} = f_{in} \times \frac{n}{m} \tag{2.25}$$

frequency multiplication factor becomes;

$$F = \frac{n}{m} \tag{2.26}$$

Maximum output frequency for DLL-based frequency multiplier is achievable for m=1 (usually is the case for most of the DLL applications). The maximum output frequency is simply;

$$f_{out} = n \times f_{ref} \tag{2.27}$$

equation (2.26) suggests that fractional multiplication can be done, in DLL-based frequency multipliers by controlling the number of delay stages, n and reference period cycles to be locked, m.

In frequency synthesizing applications, PLLs offer very high multiplication factors compared to DLLs. PLLs output frequency, so as occupied VCOs output frequency mostly determined by the used circuit topology, device speeds and limitations of oscillation theory (Barkhausen Criteria). VCOs' high frequency output could be lowered by frequency dividers and should lock to a very low frequency reference clock signal (generally crystal oscillators). This feature allows very high multiplication factors, say it 100 with 30MHz reference and 3GHz VCO. In DLLs, number of delay stages used in VCDLs directly determines multiplication factor. Number of delay stages is mostly determined by the lock range of the DLL, circuit properties and delay stage characteristic, such as minimum delay and adjustable delay of the stages. So it could be impossible to achieve high multiplication factors such as PLLs have so in DLL-based frequency synthesizer applications reference frequency should be increased in order to achieve higher output frequencies. Therefore loop components of the DLL should work higher frequencies with respect to PLLs, which hardens the design of DLLs although stability nature makes them easer to design.

Edge combining function could be implemented various way, which were took place in the literature. Basic working principle can be defined as the sum of the each delayed version of the reference clock signal. This could be done by digital logic functions AND/OR logic [Foley and Flynn, 2000 and Zhuand, 2003] or summing the phases with the aid of LC tank [Chien, G., 2000], or LC filtering of properly summing [Spataro, A. and Deval, Y., 2003]. These techniques will be explained and compared with each other in chapter 4.

It is well known that jitter accumulation phenomenon of ring oscillator VCOs results poor phase noise performance of synthesized clock signals from PLLs. Thus, But VCDLs in DLLs, introduces only buffer noise to the synthesized clock signal thus DLLs offer excellent phase noise performances over PLLs. In modern transceiver architectures, a phase noise profile of local oscillators directly determines the quality of received or transmitted signal thus affects bit error rate, BER.

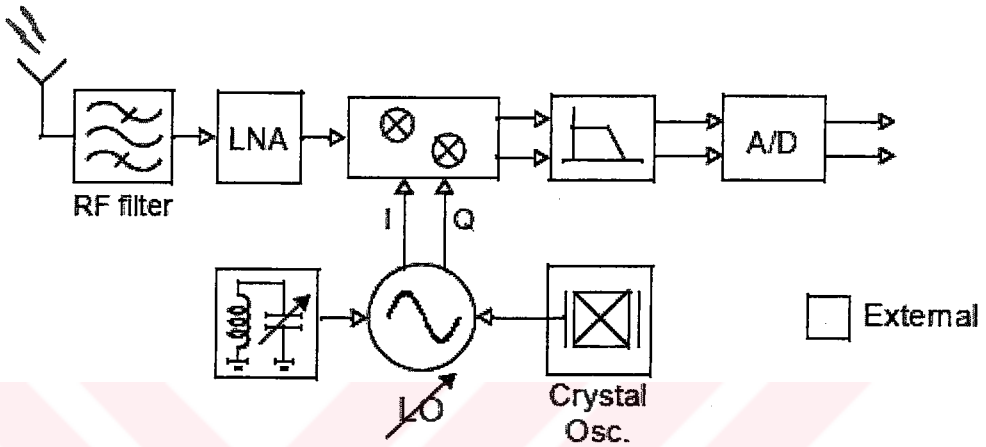


Figure 2.28 Direct conversion receiver block diagram

A direct conversion receiver (Zero-IF) architecture, shown in Figure 2.28, occupies a mixer and local oscillator, LO. Received signal from the antenna is filtered with in order to get interested frequency band and then is amplified by low noise amplifier (LNA) and the mixer multiplies the data input and LO signals producing two components, one of them is at the summed frequency of the two input and the other is at the frequency of subtraction of two inputs (downconversion). The high frequency component (summed frequency) is filtered out with following low pass filter. Interested component will go through filter and be converted to digital code in order to prepare the received signal for digital signal processing, DSP (demodulating, signal processing etc.).

It is important to have low phase noise LO signal in order to downconvert the input signal. As could be seen in Figure 2.29a, two tones present in the input of the mixer and Figure 2.29b shows LO ideal output, a dirac function. After mixing of the input and the LO output, the two tones at the input will be downconverted to lower frequencies and the unwanted tone could be eliminated with the aid of appropriate filtering processing (Figure 2.29c). If the LO output has poor phase noise performance which results skirts around the carrier frequency as could be seen in Figure 2.29d, the downconverted version of input signal will be like in Figure 2.29e. But this time it is almost impossible to distinguish the wanted and unwanted tones. Very

special filtering techniques could be applicable to these tones if the poor BER is acceptable in the application. There are very tight specifications in standard applications such as GSM, DECT etc. above examples could be applicable for other transceiver architectures too, such as heterodyne, low-IF, image-reject architectures.

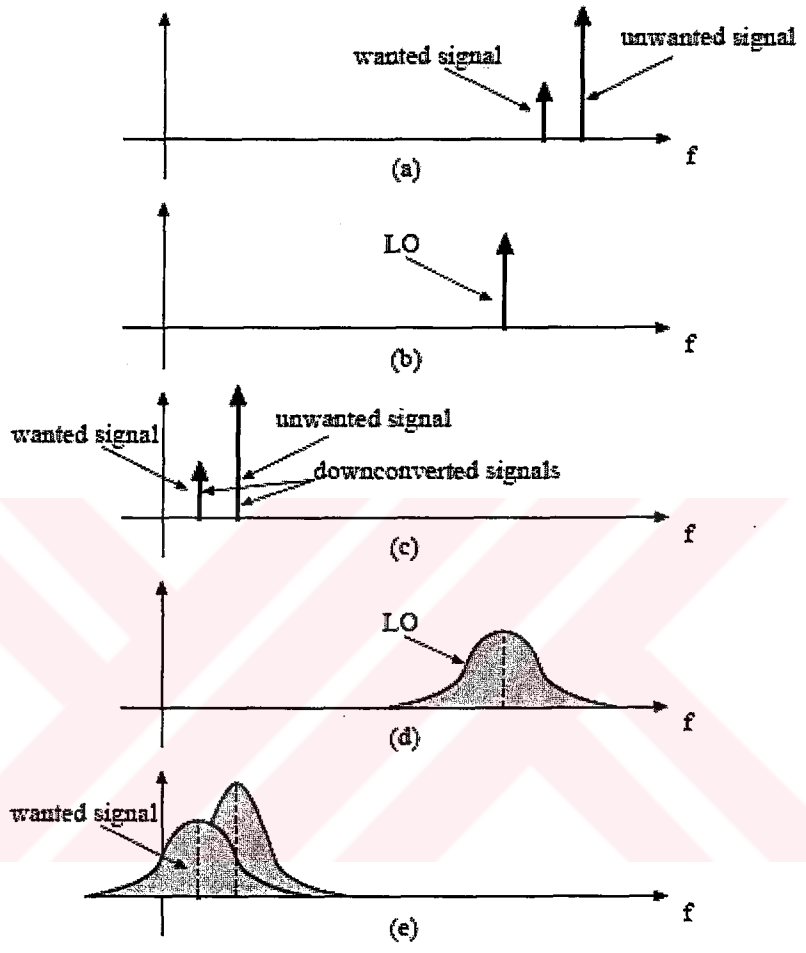


Figure 2.29 The effect of LO phase noise on downconverted signals.

Spurious tone performance of LO output is also have significant effect on receiver performances. Consider unwanted tones around the LO carrier frequency in Figure 2.29b. Mixer would respond to these spurs too. This time downconversion would occur not for just the carrier and the input but spurs and the input. Thus the unwanted tone would fall in to close-in band of wanted signal and filtering these unwanted tones could be impossible even with high-Q filters. DLL-based frequency multipliers design should involve the spur managing. These spurious tones generally occur at reference frequency around the carrier. Thus properly selected DLL reference input frequency could prevent the problems related with the spurious tones, and their levels could be lowered by proper design techniques.

It should also be noted that, most of the transceiver architectures require quadrature clock signals. DLLs offer this feature and different amount of phase shifted clock signals could be generated by properly summing, each delay cell outputs.

2.5.4 Clock and Data Recovery

High-speed serial digital data communication networks and communication standards are finding increased application in mainstream optical telecommunications. Increasing demand on serial communication systems creates a need for small and easy-to-use fiber optic receivers, key elements of which are the recovery of the clock signal embedded in the non-return-to-zero (NRZ) serial data stream and re-establishing the synchronous timing of the data using the recovered clock as the reference, shown in Figure 2.30.

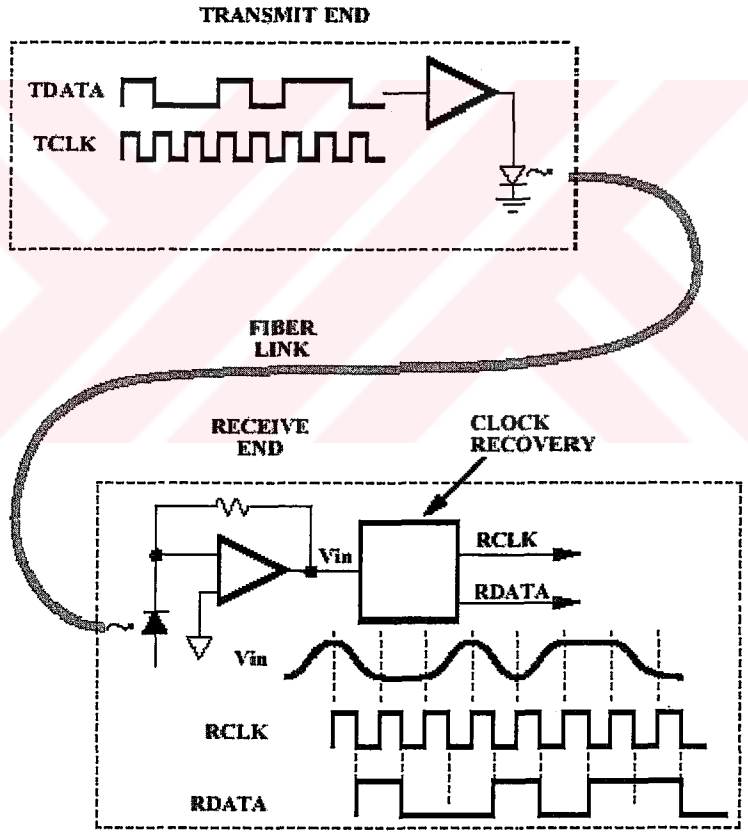


Figure 2.30 Typical fiber optic serial data transmission system.

Mostly PLLs are used in this kind of applications either with a reference clock signal or recovering clock from the data stream. But PLLs poor jitter performance brings DLL as a solution. Figure 2.31 shows basic example involving a DLL used in this kind of application. DLL would lock the two inputs of the phase detector which means that reference frequency period of delay would appear within these two inputs. If the reference frequency had been

chosen equal to the received data bit rate then the replica of the VCDL (master delay line) would equally divide the each received bit into number of delay cell (called number of TAPs in this application) because each delay line shares the same control voltage. These divided points of any bit would be sampled and a digital control unit would decide which sample is the most reliable or most clear, meaning that where to sample the ingoing signal to recover the received bit.

DLLs used in CDR applications require an external reference clock signal, whose frequency is equal to the data rate. Tracking behavior of CDR determined by the digital control unit, which is in contrast to PLLs.

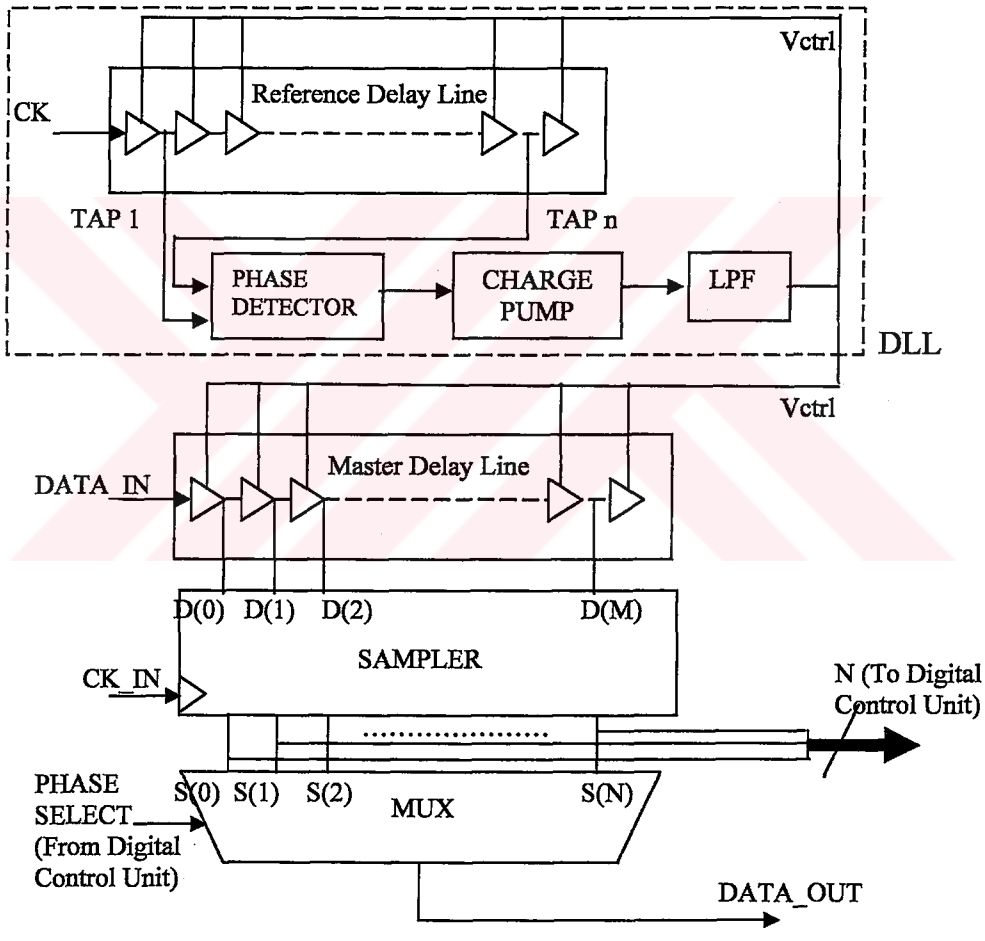


Figure 2.31 DLL used in CDR application.

2.5.5 Other Application Areas

DLLs could be used in symbol synchronization mechanism in digital communication systems such as demodulators in MODEMs, which is a kind of data recovery system. DLLs also incorporate phase detectors, which produce a phase error for its input, which enables the use

of DLLs as a phase modulator, PM, as the PLLs do. DLLs contain time information at the output of the each delay stage of the VCDL, allowing the use of the DLLs in time-to-digital converters. DLLs could also be used in RADAR systems by its controllable delay feature, which rely on finding the echo signals by comparing received signal with delayed version of transmitted signal [Paulino, N. and Serrazina, M., 2003].

3 DLL DYNAMICS AND NOISE PROPERTIES

Delay locked loop, DLL, is a unit negative feedback control system. In order to investigate the feedback system's characteristics such as stability, noise performance and noise transfer performance, DLL transfer function should be extracted from a linear DLL s-domain representation and examined. In some cases, first order s-domain model would not represent all the characteristics of a DLL such as inherent jitter performance and jitter transfer properties. Thus more complicated s-domain or discrete-time z-domain models should be developed.

Different kinds of DLLs have taken place in the literature. Figure 3.1 shows a fully digital DLL block diagram which incorporates a digital control unit in place of charge pump and loop filter, where digital control unit sets a predefined delay value for VCDL, either enabling/disabling numbers of delay stages or setting the phase shift of the delay cells with a control word according to phase difference value produced by the phase detector. Digital DLLs are suitable for megahertz range digital signal processing applications (DSPs), where the zero phase offset is not necessary but minimum achievable phase offset is enough. The minimum achievable phase offset is determined by the resolution of the control word thus the VCDL.

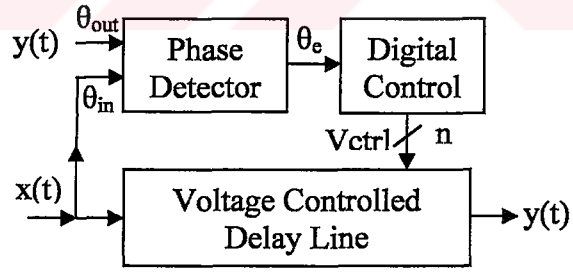


Figure 3.1 Fully "Digital" DLL block diagram.

Another version of DLL could be seen in Figure 3.2, which took interest in recent years in frequency synthesizing applications [Ramin, 2002 and Ye, 2003]. The main idea is combining the high multiplication factors of PLLs and the excellent phase noise performance of DLLs by controlling the loop with a digital unit, whether selecting ring oscillator configuration of VCDL or delay chain configuration. Ring oscillator configuration produces high frequency clock signal and this output is aligned to a periodic clean reference signal in order to reset the

noise memory of the ring oscillator, which prevents the jitter accumulation phenomenon, thus producing a low phase noise output as DLLs do.

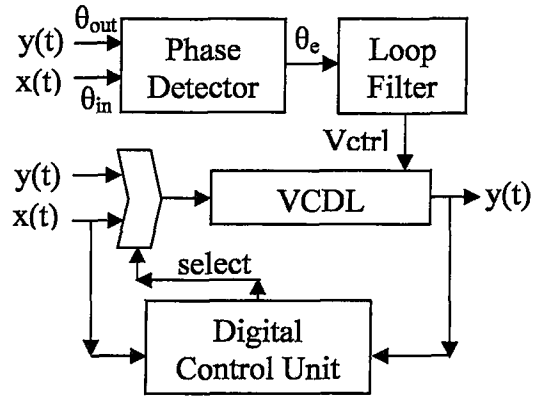


Figure 3.2 Re-circulating DLL block diagram.

The above two versions of DLL is off concern of this thesis, but the achieved results for analog DLL can be applicable to them.

DLLs can be divided into two categories, which can be called Type-I and Type-II, according to different application areas resulting different jitter transfer characteristics (Figure 3.3). A typical application for Type-II as a skew canceller is shown in Figure 3.4, where all DLLs lock their outputs to a clean reference.

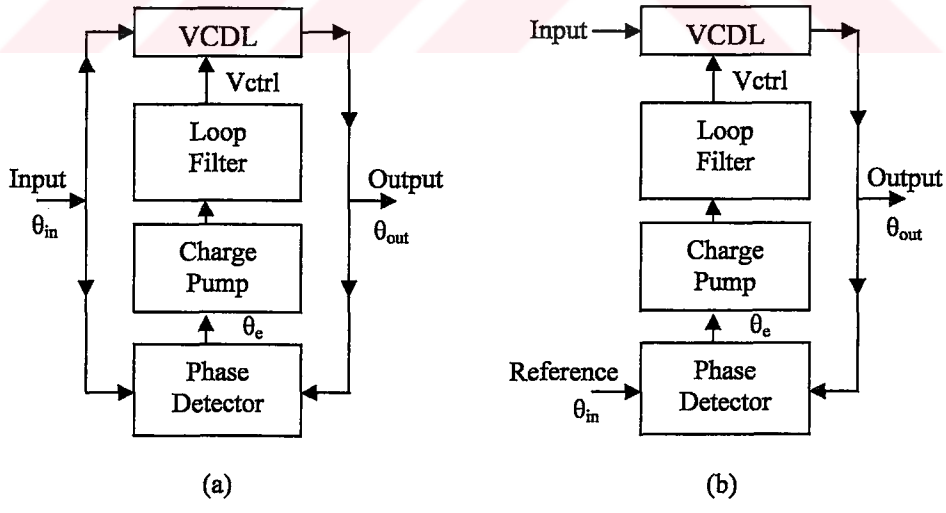


Figure 3.3 DLL block diagrams (a) Type-I and (b) Type-II

In a Type-I DLL, the reference signal is compared with the delayed version of itself, widely used in clock skew cancellation, multiphase clocking and frequency multiplication applications. In a Type-II DLL, the reference is compared with the delayed version of an uncorrelated clock signal, which architecture is widely used in CDR and skew cancellation

applications. This feature relates difference noise transfer characteristics because one compares the input and its derived version seen at the output and the other corrects its output to a clean reference signal, resulting Type-I DLLs having "jitter peaking" as PLLs does and can never be eliminated. Jitter peaking refers to the amplification of jitter from an input to an output over a certain frequency band and is an important metric in systems where multiple PLLs or DLLs are cascaded, such as in clock repeaters and clock distribution networks. This phenomenon of Type-I DLLs, which is used more frequently than the Type-I in practice, have not been realized until last year [Edward Lee, 2003]. Thus jitter peaking phenomenon of the Type-I DLLs should be examined carefully by modeling its nature.

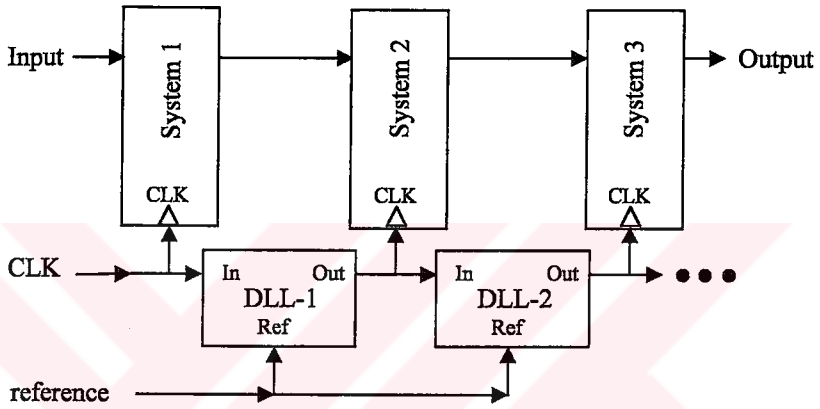


Figure 3.4 Type-II DLL in skew cancellation application

In chapter 2, basic definitions and construction of DLLs has been discussed and each loop components' working principles and transfer functions have been given. Also DLL application areas, which make DLL block diagram to be modified, have been presented in chapter 2.5. These modifications could result different DLL characteristics and should be examined carefully in order to keep in hand the excellent features of DLLs, such as stable nature, noise performance etc.

Following section describes linear s-domain modeling, z-domain representation of Type-I DLL where s-domain becomes incapable and noise properties of DLLs.

3.1 Small-signal AC Model

Simplified block diagram of DLL loop shown in Figure 3.5a can be redrawn with the small-signal AC transfer functions of the building blocks given in previous chapter, which could be seen in Figure 3.5b. In this linearized model, in case of using sequential phase detector with a

charge pump, the combined transfer function of these is represented with K_{PD_CP}, F(s) is the loop filter transfer function and K_{VCDL} is the voltage controlled delay line gain.

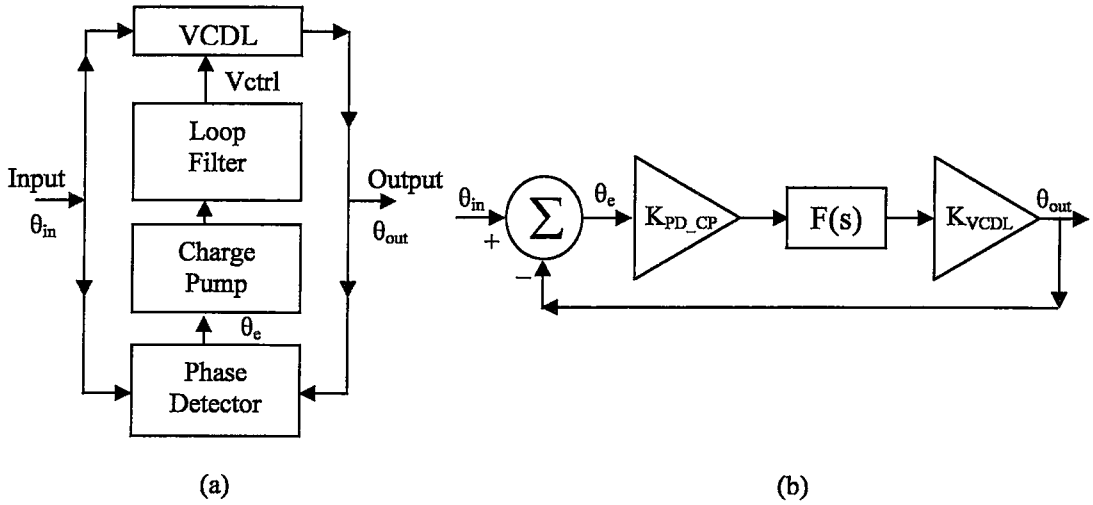


Figure 3.5 s-domain representation of DLL loop

Figure 3.5b can be easily recognized as a simple feedback system with unit feedback. The open-loop gain is

$$G(s) = K_{PD\_CP}.F(s).K_{VCDL} \tag{3.1}$$

When the loop is in a steady-state locked condition, the s-domain phase transfer function from input to the output can be written using Mason's theorem. The closed-loop transfer function is

$$\frac{\theta_{out}}{\theta_{in}} = H(s) = \frac{G(s)}{1+G(s)} = \frac{K_{PD\_CP}.K_{VCDL}.F(s)}{1+K_{PD\_CP}.K_{VCDL}.F(s)} \tag{3.2}$$

Recognize that the loop filter is formed as first order with only a capacitor, a pole at zero, forming a perfect integrator. Transfer function of the loop filter is

$$F(s) = \frac{K_{LF}}{s\tau_p} = \frac{K_{LF}}{sC_p} \tag{3.3}$$

where K_{LF} is loop filter gain and C_p is the capacitor value and in case of passive loop filter implementation K_{LF}=1. It should be noted that for clarity, from chapter 2, $K_{PD\_CP}=I_{cp}/2\pi$ and K_{VCDL}=(phase deviation)/(control signal). Now, equation (3.1) becomes;

$$G(s) = \frac{K_{PD\_CP}.K_{VCDL}}{sC_p} \tag{3.4}$$

Then closed-loop response is

$$H(s) = \frac{\theta_{out}}{\theta_{in}} = \frac{\omega_n}{s+\omega_n} = \frac{\frac{K_{PD\_CP}.K_{VCDL}}{C_p}}{s+\frac{K_{PD\_CP}.K_{VCDL}}{C_p}} \tag{3.5}$$

This equation suggests a first order loop transfer function, which is inherently stable. Unlike the small-signal AC model for typical PLL, a minimum of a second order transfer function is required and no stability precautions required in a DLL.

Since the transfer function is inherently stable, wider loop bandwidth can be used, in order to decrease the lock time, faster acquisition time and as well as the use of smaller loop filter capacitors facilitating integration. It is also important that similar to PLL case, the small-signal AC model is valid when the loop bandwidth is much smaller than the phase detector comparison frequency (generally 1/10). Therefore upper limit for loop bandwidth is determined by the DLL operating frequency and noise behavior of DLL.

Assuming the DLL loop has infinite bandwidth, which guarantees signals at input and output of the delay chain are perfectly in-phase, the thermal-noise-induced random timing error associated with each delay stage determines the noise performance of the DLL. In reality, the loop has a finite bandwidth, which limits the loop response time. A slow acting variation in the control voltage, which causes the correlated timing error for delay stages, is corrected by the loop. These variations generally prolong or shorten the time delay of delay stages uniformly. However, a fast acting variation whose frequency might be higher than the loop bandwidth cannot be corrected by the loop, such as power supply and control voltage noise. When the timing errors for delay stages are un-correlated, the total timing error at the output of the delay chain no longer carries the timing error information of each individual delay stage. Thus, the loop is able to correct only the average timing error seen at the output that results an amount of phase deviation of each delay stage output, which causes serious problems for multiphase clocking and frequency synthesizing applications, regardless of the loop bandwidth, as explained in chapter 2.5.

It should be noted that although using a first order loop filter, a pole at zero, second pole could be introduced to the system either on purpose or inevitable circuit level realization practice. Considering a second pole at ω_p, transfer function of the DLL (equation 3.5) becomes;

$$H(s)=\frac{\theta_{out}}{\theta_{in}}=\frac{1}{\frac{s^2}{\frac{\omega_p.K_{VCDL}.K_{PD\_CP}}{C_p}}+\frac{s}{\frac{K_{VCDL}.K_{PD\_CP}}{C_p}}+1} \tag{3.6}$$

if the second pole is at very high frequencies, $\omega p \rightarrow \infty$, equation (3.6) reduces to equation (3.5). This pole has to be considered carefully by means of the DLL operating frequency and the loop bandwidth. First order DLL transfer function does not contain a zero, thus suggesting no jitter peaking phenomenon, but because of circuit level realization of the components, a "parasitic zero" could raise. Linear DLL model should be carefully updated in implementation step of the DLL for a complete analysis.

In order to determine the noise behavior of the DLL, several additive noise sources have to be included in the DLL linear model, and their effects on the output should be examined. Figure 3.6 shows possible error sources for each node of the DLL block diagram, which could affect the DLL output noise power.

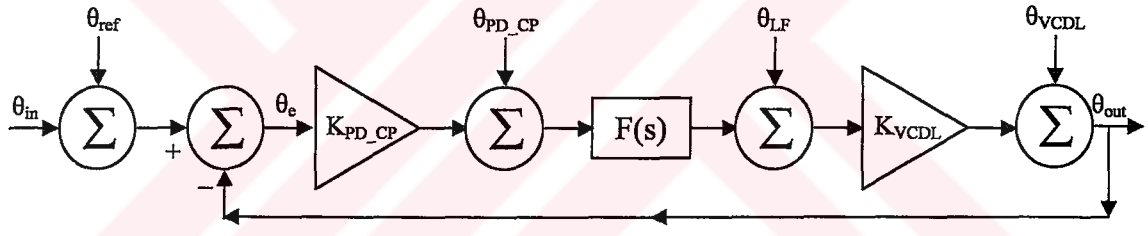


Figure 3.6 s-domain representation of DLL with additive noise sources

It is well known that the one-side input noise power density shaped with the transfer function of the system, H(jω), determines output power spectral density of a linear time-invariant system. This could be written as;

$$S_{out}(\omega)=S_{in}(\omega).|H(j\omega)|^2 \tag{3.7}$$

The overall output noise power could be written in addition of each noise sources' effects to the output in a linear system. Thus total DLL output noise power is;

$$S_{\theta_{out}}(f)=S_{\theta_{ref}}(f).|H_{ref}(j2\pi f)|^2+S_{\theta_{PD\_CP}}(f).|H_{PD\_CP}(j2\pi f)|^2+S_{\theta_{LF}}(f).|H_{LF}(j2\pi f)|^2 \\ +S_{\theta_{VCDL}}(f).|H_{VCDL}(j2\pi f)|^2 \tag{3.8}$$

each nodes transfer function has to be written for a complete noise analysis.

Reference noise is one of the dominant noise sources in DLLs. The closed-loop response of a DLL to a reference noise signal is;

$$H_{ref}(s) = \frac{\theta_{out}}{\theta_{ref}} = \frac{K_{PD\_CP}.K_{VCDL}.F(s)}{1+K_{PD\_CP}.K_{VCDL}.F(s)} \tag{3.9}$$

which is same as the closed-loop transfer function of a DLL. The characteristic of the transfer function is directly determined by loop filter transfer function thus loop filter is formed by only a capacitor, $F(s)=1/sC_p$, the reference noise transfer function has low-pass characteristic as the loop filter does.

Phase detector does not contribute noise to the output when the loop is locked and can be safely ignored. But in this analyses phase detector and charge pump is combined thus noise transfer function of this block should be taken into account. That is

$$H_{PD\_CP}(s) = \frac{\theta_{out}}{\theta_{PD\_CP}} = \frac{K_{VCDL}.F(s)}{1+K_{PD\_CP}.K_{VCDL}.F(s)} \tag{3.10}$$

which has a low-pass characteristic for $F(s)=1/sC_p$ as the case.

Loop filter output noise contribution to output is

$$H_{LF}(s) = \frac{\theta_{out}}{\theta_{LF}} = \frac{K_{VCDL}}{1+K_{PD\_CP}.K_{VCDL}.F(s)} \tag{3.11}$$

for $F(s)=1/sC_p$ it has high-pass characteristic. But loop-filter contains only a capacitor and does not contribute any noise (if the loop filter contains a resistor, it produces thermal noise and thus should be calculated).

The most important noise source is the VCDL noise considering loop components. Thus VCDL output noise transfer function is;

$$H_{VCDL}(s) = \frac{\theta_{out}}{\theta_{VCDL}} = \frac{1}{1+K_{VCDL}.K_{VCDL}.F(s)} \tag{3.12}$$

which has a high-pass characteristic, as the VCO of a typical PLL. Loop will reduce the low frequency noise component of VCDL but high frequency part will be directly coupled to output of the DLL. Compared to VCO, VCDL introduces only buffer noise rather than noise accumulation in every cycle. This is why the VCDL is the most important noise source of the DLL and DLLs perform excellent phase noise characteristic compared to PLLs.

At a glance, while keeping in mind that phase detector and loop filter introduce ignorable amount of noise, combining the equation (3.8) and the noise transfer functions of each individual noise sources, minimizing the loop bandwidth will reduce the reference noise contribution but VCDL output contribution at frequencies above cutoff frequency will not be attenuated. Keeping in mind that VCDL experiences only cascaded buffer noise and shows no noise memory, loop bandwidth can be arranged according to the reference noise contribution, which might likely be larger than the VCDL noise contribution except in case of using crystal oscillator at the reference input signal.

3.2 Discrete-time Model

In order to determine consequences of sampling nature of the DLL, discrete-time z-domain model should be generated. As mentioned before, some aspects of DLLs like effect of loop delay, defined as the time elapsed from the generation of a phase error signal, θ_e, until the corresponding clock phase shift is produced after the loop delay time, and jitter peaking phenomenon should be carefully investigated. These effects could be integrated with linear s-domain analysis too, but discrete-time domain analysis would make these effects clear.

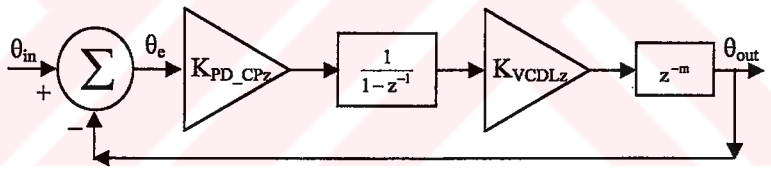


Figure 3.7 Discrete-time model of a DLL

A simple z-domain could be formed as seen in Figure 3.7 [Liu, A. and Lee, J., 1999]. Subscripts "z" refers the z-domain form of the corresponding stages, those will include sampling frequency term. Phase detectors' operation could be model with an adder, $\theta_e=\theta_{in}-\theta_{out}$. Gain of the phase detector could be combined with charge pump as the case in s-domain representation. These blocks were represented with K_{PD_CPz} gain stage and a perfect z-domain integrator, $1/(1-z^{-1})$. Including sampling nature and reminding $T_{ref}=1/f_{ref}=1/f_{clk}$;

$$K_{PD\_CPz} = \frac{I_{cp}}{\omega_{clk} C_p} = \frac{I_{cp}}{2\pi C_p}.T_{ref} \tag{3.13}$$

VCDL is formed with a gain stage, K_{VCDLz} that is equal to K_{VCDL} and a sampler z^{-m}. z^{-m} block represents the loop delay, T_{loop}, which can be considered as the loop reaction time to a phase difference value either dominated by delay stage nature itself or some delay introduced to the

feedback loop shown in Figure 2.21b as a clock driver stage. Thus "m" value would be understood as the ratio of the loop delay with respect to comparison time period, which is the integer part of $(1+T_{loop}/T_{ref})$. If we define loop stability constant, K, as;

$$K = K_{PD\_CPz}.K_{VCDLz} \tag{3.14}$$

Phase transfer function from input to output of the DLL is;

$$H(z) = \frac{\theta_{out}(z)}{\theta_{in}(z)} = \frac{K}{z^m - z^{m-1} + K} \tag{3.15}$$

The stability of the general transfer function derived above should be examined carefully according to "m" value, which could vary for different kind of applications of DLL.

Also Equation (3.15) could say about "jitter peaking", but a dedicated discrete time model for this phenomenon should be useful [Edward Lee, 2003], which has to be included the fact that θ_{out} is derived from θ_{in}, and the phase detector produces an error signal for previous state of the VCDL output, shown in Figure 3.8.

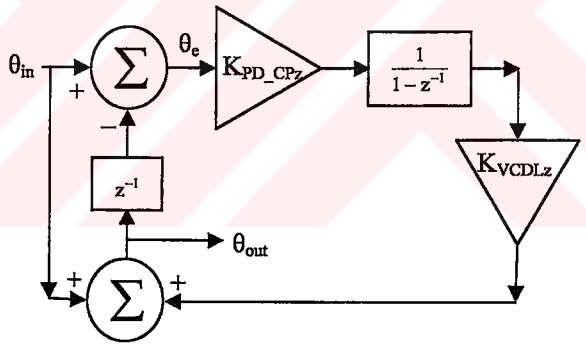


Figure 3.8 Modified z-domain model of Type-I DLL

Combined phase detector and charge pump gains are given in equation (3.13). Here, as a special case of z^{-m}, m=1 and could be included in VCDL gain with a new definition of VCDL gain as phase shift per control signal per cycle. By doing so jitter transfer should be given as;

$$\frac{\theta_{out}(z)}{\theta_{in}(z)} = \frac{(1+K_{PD\_CP}.K_{VCDL})z-1}{z-(1-K_{PD\_CP}.K_{VCDL})} = \frac{(1+K)z-1}{z-(1-K)} \tag{3.16}$$

which contains a pole at (1–K) and a zero at 1/(1+K). For nonzero stability constant K, jitter peak can never be eliminated because of zero. The maximum jitter peaking can be calculated with z=–1 (at half of the sampling frequency) because of the sampling nature of the system, jitter above the Nyquist frequency gets aliased down to the Nyquist bandwidth. Thus,

$$\text{JitterPeaking} = P = \frac{2+K}{2-K} \tag{3.17}$$

smaller loop bandwidth would reduce jitter peaking but increase acquisition time of the DLL.

Jitter peaking occurs in Type-I DLL because it cannot distinguish between input clock jitter and output clock jitter. For example, when the phase detector sees θ_{in} lag θ_{out}, it could mean that θ_{in} has a sudden lagging jitter or that the delay between θ_{in} and θ_{out} suddenly became smaller. The former requires that the delay be decreased and the latter increased in order to prevent any jitter in θ_{out}. The two scenarios have conflicting requirements. Since the Type-I DLL adjusts the delay between θ_{in} and θ_{out}; the latter must be done in order to prevent positive feedback. This means that any sudden jitter in θ_{in} is temporarily amplified until this jitter propagates to θ_{out} and the loop reacts in the correct direction.

It also should be noted that, a z-domain pole or zero, z_o, could be converted to an s-domain pole or zero ω_o by

$$z_o = e^{-\omega_o T_i} \qquad (\text{for } 0 < z < 1) \tag{3.18}$$

Achieved results (equation 3.17) should be considered with the reference noise transfer function and the VCDL output noise transfer function (equation 3.8 and 3.12 respectively). Minimum DLL loop bandwidth will both reduce the reference noise contribution and jitter peaking but VCDL inherent noise contribution and the lock time will be higher.

3.3 Timing Jitter and Phase Noise

3.3.1 Introduction

Timing Jitter can be defined as the unwanted time deviations with respect to ideal crossing point of a signal. Time deviations can cause from noise sources that affects the signal, or the circuits' inherent noisy behavior that affects the ingoing signal. Timing jitter also manifests it self in frequency domain. The affect of the amplitude and phase noise can be understood from Figure 3.9 where an ideal sine wave is exposed to noise resulting amplitude variations and phase noise resulting a random deviation of the zero crossing of the signal thus resulting a frequency deviation of the signal. In frequency domain an ideal sine wave manifest itself with a delta function (dirac), but in case of the sine wave is exposed to noise, a noise floor from the amplitude noise and noise skirts around the carrier is observed.

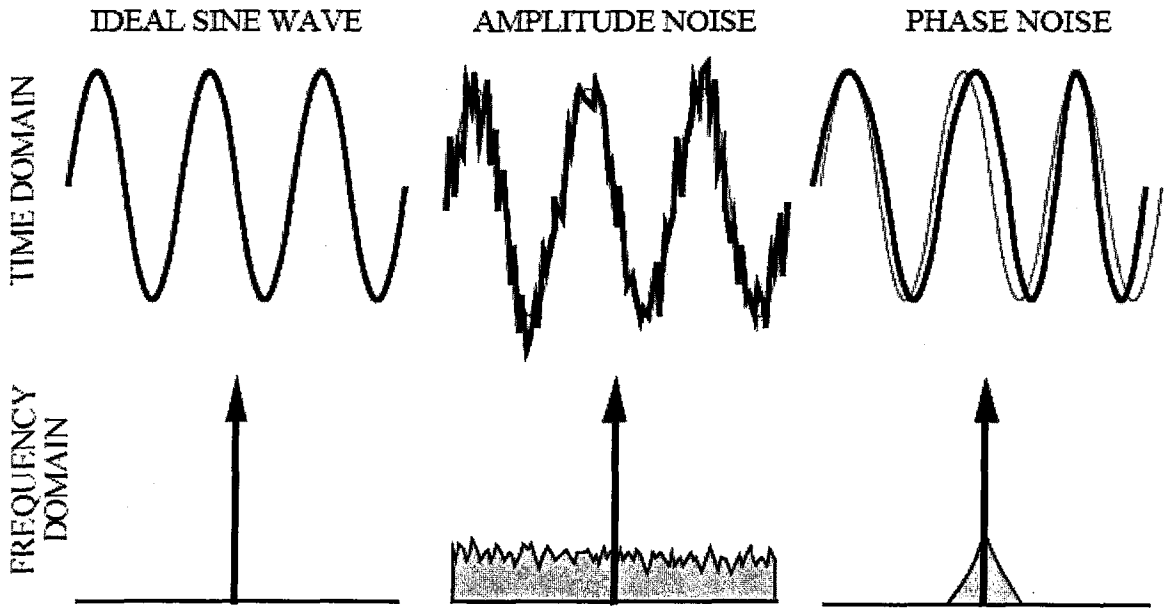


Figure 3.9 Jitter in time and frequency domain

Consequences of the timing jitter in various applications are explained in section 2.5 in detail. Thus it is important to determine the noise sources and their effects to the total timing jitter in a basic buffer circuit as a starting point. Also it should be noted that, most important building block of a DLL is the VCDL, which is constructed with cascaded buffers when calculating the total output jitter.

Timing jitter is defined in rms fashion. Also peak-to-peak, cycle-to-cycle, unit interval etc, fashions where the choice likely depends on the application areas, can be derived from rms jitter.

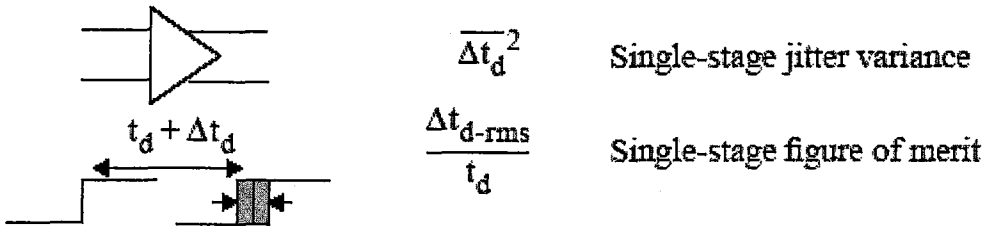


Figure 3.10 Illustration of timing jitter in an individual delay stage

Analyses of a buffer will correspond to a delay cell, which will be used in VCDL. Consider a buffer circuit whose input signal experiences a step (Figure 3.10). Buffer will pass through the transition seen in the input with a time delay but the buffer experiences a delay uncertainty result of timing errors caused by circuit noise. The amount of the uncertainty is defined as the timing jitter. The timing error is usually zero mean, and Gaussian, with

variance of $\overline{\Delta t_d^2}$ (σ^2). A figure of merit can be defined relating the jitter and time delay [Weigandt, C., 1998].

In a buffer, the independent timing errors, which accompany each cycle, perturb the output phase, but do not change the period of the time-base for example which produces the next cycle of oscillation in frequency multiplier applications. In this sense, they produce "white phase noise". This is illustrated in Figure 3.11. The height of the phase noise floor in such a case is proportional to the jitter variance of the delay stage. This figure shows the power spectrum of the phase fluctuations, $S_\theta(f)$. The power spectrum of a signal passed through such a buffer, $S_x(f)$, with a reasonably low noise floor, is approximately the same as the input spectrum with a white phase noise floor added [Weigandt, C., 1998].

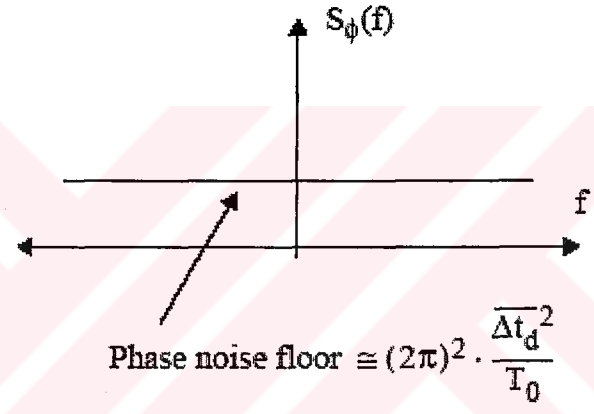


Figure 3.11 Buffer phase noise spectrum.

Timing jitter in clock buffers also translates into phase noise when viewed in the frequency domain. It well known that the phase noise introduced by a clock buffer is different than that introduced in an oscillator. For the oscillator case, timing jitter introduced with each cycle of oscillation corrupts the instantaneous frequency of the oscillator. The result was shown to be phase noise sidebands, which fall as $1/\omega^2$. In the clock buffer case, timing jitter corrupts the phase of the output signal, but does not change the instantaneous frequency of the source, which drives it. This can be shown to create a white phase noise spectrum ($1/\omega^0$).

The introduction of timing jitter to a clock source and the resulting phase noise are illustrated in Figure 3.12. A timing error with variance is added to each edge in the output signal. If just the thermal noise sources in the buffer circuit are considered, then noise from once cycle of oscillation to the next is uncorrelated. Samples of the output phase error as a function of time might appear as in figure 3.13, where the variance of each sample given by,

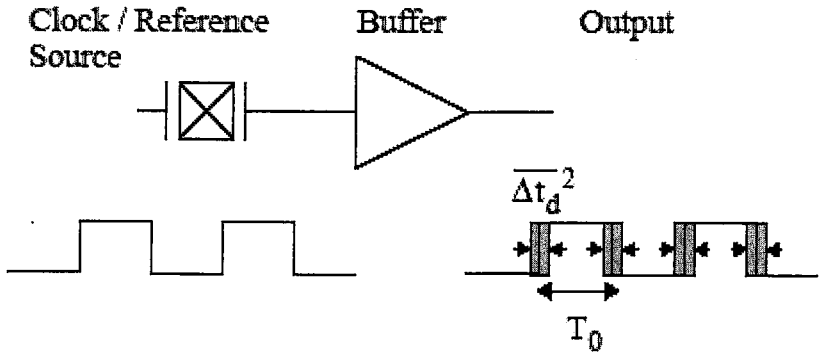
$$\sigma_\theta^2 = (2\pi)^2 \frac{\overline{\Delta t_d}^2}{T_o^2} \tag{3.19}$$

If the phase error is actually considered to be zero in between the time instances T_0, $2T_0$, ... , then there are problems related to the analysis of non-bandlimited continuous time white noise. The autocorrelation function for this noise process and the output power spectral density (which is the Fourier transform of the autocorrelation function) can be more readily found with a further assumption for the value of the phase noise between "samples". If the phase error samples are assumed to be Nyquist rate samples of a white noise process bandlimited to $(-f_o/2, f_o/2)$, then a reasonable answer can be attained. The result is a band-limited approximation to the phase noise with a power spectral density of height σ_θ^2/f_o in band, as pictured in Figure 3.12.

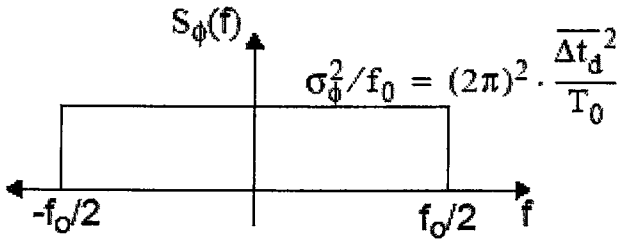
This means that phase noise in band is white with power spectral density;

$$S_\theta(f) = \frac{\sigma_\theta^2}{f_o} = (2\pi)^2 \frac{\overline{\Delta t_d}^2}{T_o} \tag{3.20}$$

In order to reduce phase noise, it is important to determine the noise sources and their effects, and then manipulations on design parameters have to be made. It should also be noted that, phase noise floor for a given output jitter is higher for higher frequency sources.



(a)



(b)

Figure 3.12 Timing jitter in clock buffers (a) addition of timing jitter to output signal (b) resulting output phase noise spectrum

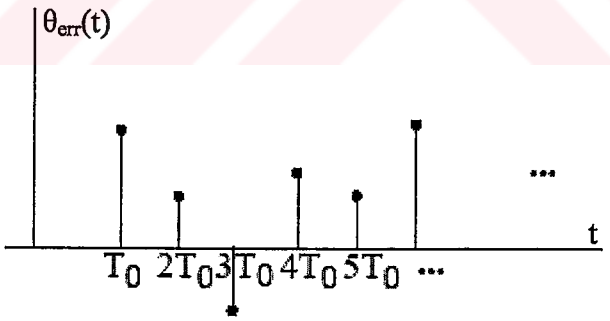


Figure 3.13 Phase error as a function of time.

3.3.2 Noise Sources in a Differential Pair

The noise source that is the major contributor to jitter depends to a large extent on what kind of buffer is used as the delay element for VCDL. For illustration, the simple delay stage shown in Figure 3.14 will be discussed. In practice, emitter followers are usually used to buffer the collector voltages. For now, we will consider only noise sources in the differential pair (chapter 4).

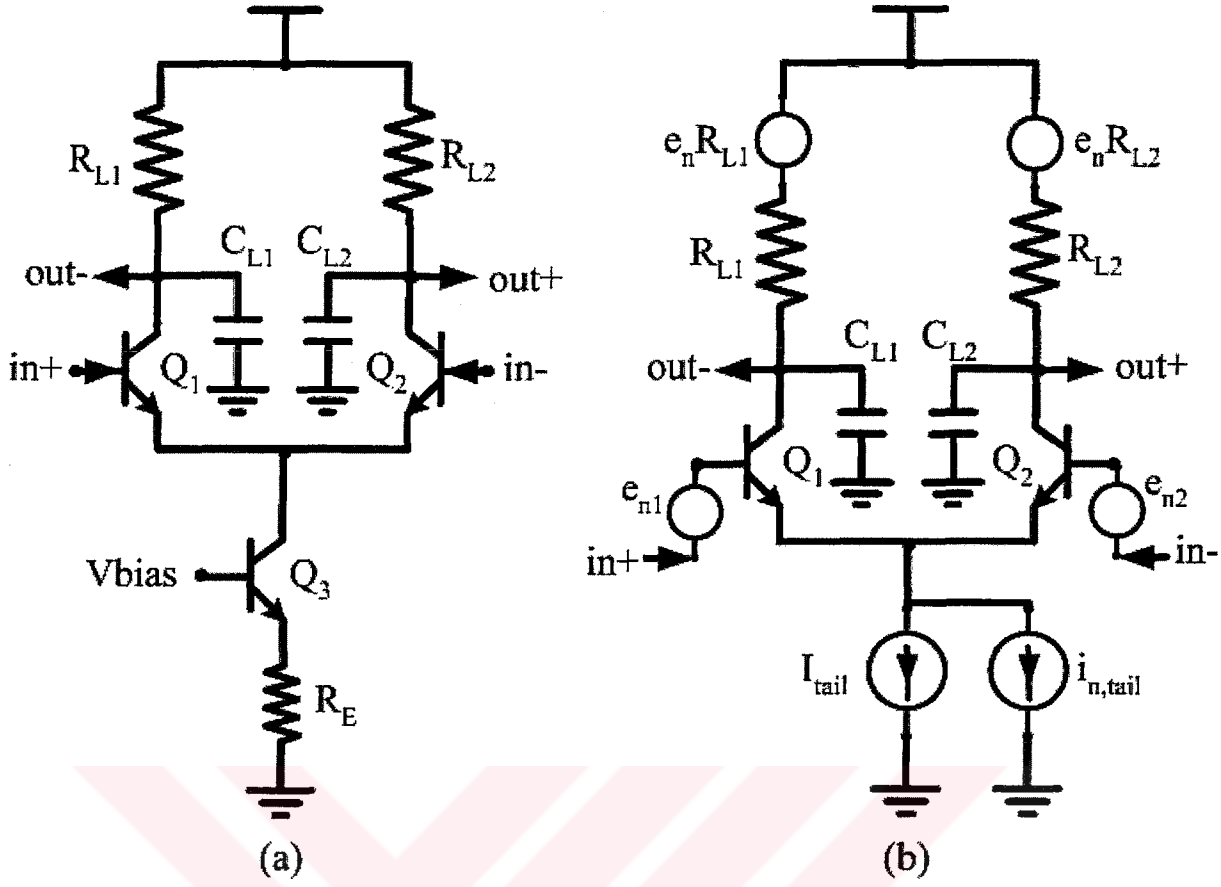


Figure 3.14 Differential pair with representative noise sources

The input voltage V_{in} causes differential pair Q_1/Q_2 to steer the tail current I_{tail} to one of the collector loads, R_{L1} or R_{L2}. Capacitors C_{L1} and C_{L2} represent wiring stray, junction, and any explicit capacitances that may be present at the collector node. The differential output is taken between the two collectors. Following are some of the possible noise sources to be considered. In each case a distinction will be made as to whether the noise source is fundamental (cannot be eliminated) or not (could in principle be eliminated through appropriate design).

Thermal noise in collector load is always present and imposes a lower limit on achievable jitter. These noise sources are represented by e_nR_{L1} and e_nR_{L2} in Figure 3.14. The sources appear directly at the output, but are bandlimited by the $R_{L1}\times C_{L1}$ and $R_{L2}\times C_{L2}$ poles. This is a fundamental source of jitter that cannot be eliminated.

Noise is also present in the tail current of the differential pair. This is represented by noise source $i_{n,tail}$ in Figure 3.14. The type of noise depends on the nature of the current source. If the tail current source is degenerated (as shown with R_E in Figure 3.14), the output noise will be dominated by the thermal noise of the degeneration resistor. If not, the noise is dominated

by the shot noise of the DC current I_{tail} [Bilotti, A., and Mariani, E., 1975]. When V_{in} is large enough to fully switch the differential pair, the current noise is passed to the output, but is bandlimited by the either the $R_{L1}\times C_{L1}$ or $R_{L2}\times C_{L2}$ pole. When V_{in} is small, the differential pair is approximately balanced. The tail current noise is a common mode error and does not affect the differential V_{out}. Tail current noise is also a fundamental source of jitter that cannot be eliminated; only changed by changing the current source.

There is also thermal noise in series with the inputs of the differential pair. This is represented by noise sources e_{n1} and e_{n2} in Figure 3.14. This noise is due to thermal noise of the Q_1/Q_2 transistor base resistances [Gray, P. R., and R. G. Meyer, 1984] as well as other wideband noise sources going back to V_{out} of the preceding stage of the ring. The thermal noise is sampled by the switching action of the differential pair. This type of behavior is seen whenever high gain is used to sharpen a threshold crossing [Verhoeven, C.]. These noise sources only contribute error to the output when the input signals cross through the active region of the differential pair. The voltage noise at the input, through the transconductance of the differential pair, creates a current noise at the output, which is integrated on C_{L1} and C_{L2}. This is another fundamental source of jitter: it cannot be eliminated but can be reduced, for example by using large geometry transistors to reduce base resistance.

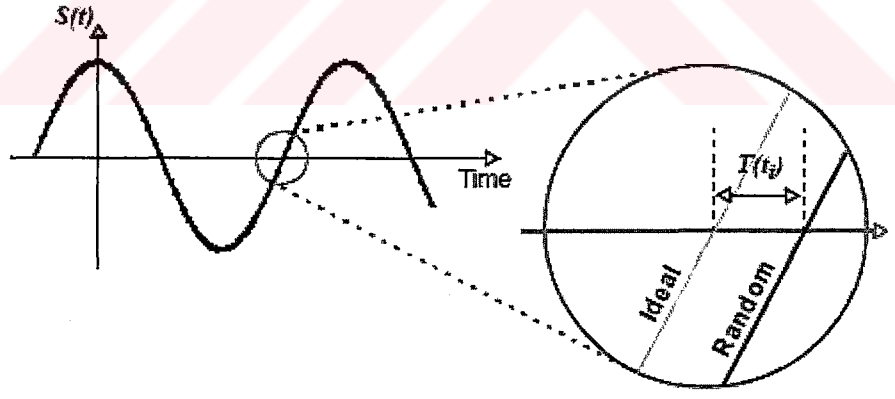


Figure 3.15 Timing uncertainties of a sine wave.

Each noise sources can be combined in rms fashion in order to predict the output jitter of the stage shown in Figure 3.14. Timing uncertainties of a sinusoidal signal can be related using "first crossing approximation".

3.3.2.1 Load Resistor Thermal Noise

First thermal noise contribution of load resistor has to be calculated using the approximation that is timing variations are equal to voltage variations and slew rate ratio at the zero crossing point (Figure 3.15). Assuming $C_{L1}=C_{L2}=C_L$ and also represents all parasitic capacitances, seen in the Figure 3.14, slew-rate can be defined as;

$$\text{SlewRate} = \frac{I_{tail}}{C_L} \tag{3.21}$$

If we assume the noise to be much less than the exponential signal, standard deviations of time and voltage errors σ_t and σ_v are also related by the slew-rate. That is;

$$\sigma_t = \frac{\sigma_v}{\text{SlewRate}} \tag{3.22}$$

The standard deviation of the differential voltage error is simply the root sum of the individual standard deviations σv1 and σv2. These are given by the Johnson noise equation

$$\sigma_v = \sigma_{v1} = \sigma_{v2} = \sqrt{4kTRB} \tag{3.23}$$

where R is the resistance and B the effective noise bandwidth. For a single pole circuit, the noise bandwidth is given by the 3-dB bandwidth multiplied by π/2 [Shanmugan, 1988];

$$B = \frac{\pi}{2}\frac{1}{2\pi RC} = \frac{1}{4RC} \tag{3.24}$$

Substituting (3.24) into (3.23) and in our case $C=C_{L1}= C_{L2}= C_L$, gives the well known result;

$$\sigma_{v1} = \sigma_{v2} = \sqrt{\frac{kT}{C}} = \sqrt{\frac{kT}{C_L}} \tag{3.25}$$

and for differential voltage (3.25) becomes;

$$\sigma_v = \sqrt{\frac{2kT}{C_L}} \tag{3.26}$$

Using (3.26) and (3.21) in (3.22) gives for the standard deviation of timing error, which is called jitter. That is,

$$\sigma_t = \frac{\sigma_v}{\text{SlewRate}} = \frac{\sqrt{\frac{2kT}{C_L}}}{\frac{I_{tail}}{C_L}} = \sqrt{\frac{2kTC_L}{I_{tail}^2}} \tag{3.27}$$

Reminding the differential pair delay [see chapter 4.3.1 and equation (4.11) for derivation] and using same notation here;

$$T_d = \ln(2).R_L.C_L \tag{3.28}$$

if we use the figure of merit that is normalized timing errors, in rms fashion;

$$\kappa = \frac{\sigma_t}{\sqrt{T_d}} = \frac{\sqrt{\frac{2kTC_L}{I_{tail}^2}}}{\sqrt{\ln(2).R_L.C_L}} = \sqrt{\frac{2}{\ln(2)}}.\sqrt{\frac{kT}{I_{tail}^2.R_L}} \cong 1.699.\sqrt{\frac{kT}{I_{tail}^2.R_L}} \tag{3.29}$$

κ has dimensions of $\sqrt{sec}$, and from (3.29) we see that this comes about by taking the square root of an energy (kT) divided by a power ($I_{tail}^2 .R_L$). The rms thermal energy kT represents an uncertainty in the energy of the collector load. $I_{tail}^2 .R_L$ represents the DC power dissipation (energy flow) in the collector load. The intuitive meaning of (3.29) is that it characterizes the stage's ability to resolve time (jitter) by an energy uncertainty (kT) as a fraction of the energy flow over time ($I_{tail}^2 .R_L$). Equation (3.29) also indicates that jitter is improved by increasing the DC power dissipation.

3.3.2.2 Tail Current Noise

When the differential pair in equilibrium, tail current noise does not affects the differential output voltage but manifest itself in common mode level. Input pair switches tail current noise $i_{n,tail}$, each load resistors depending on the input signal and thus noise current cause an error voltage on the output.

Consider a switching instant at t=0. Prior to switching, the tail current and the noise current both flow through to R_{L1}. The current noise density in drops across R_{L1} to give a voltage noise density, which integrated over the noise bandwidth (3.24) $1/4R_LC_L$ gives a standard deviation of $\sigma_{vn1}(t<0)$ as,

$$\sigma_{vn1}(t<0) = \frac{i_{n,tail}}{2}\sqrt{\frac{R_L}{C_L}} \tag{3.30}$$

when the switch is thrown at t=0, noise no longer affects v_{n1}, which begins an exponential decay with time constant R_LC_L. The standard deviation of v_{n1} for t>0 therefore has the form of a sampled noise term, decaying exponentially, which is;

$$\sigma_{vn1}(t<0)=\frac{i_{n,tail}}{2}\sqrt{\frac{R_L}{C_L}}.e^{\frac{-t}{R_LC_L}} \tag{3.31}$$

At the same time as v_{n1} begins its exponential decay, the other side,v_{n2} begins growing. Analysis shows that, assuming in white, the standard deviation of v_{n2} for t>0 is given by [McNeill, J.A., 1994],

$$\sigma_{vn2}(t>0)=\frac{i_{n,tail}}{2}\sqrt{\frac{R_L}{C_L}}.\sqrt{1-e^{\frac{-2.t}{R_LC_L}}} \tag{3.32}$$

in order to find differential output voltage standard deviation, (3.31) and (3.32) has to be summed. This simply results,

$$\sigma_v(t)=\frac{i_{n,tail}}{2}\sqrt{\frac{R_L}{C_L}} \tag{3.33}$$

standard deviation of timing uncertainty from (3.22) and (3.21) becomes,

$$\sigma_t=\frac{\sigma_v}{\text{slewrate}}=\frac{i_{n,tail}}{2}\sqrt{\frac{R_LC_L}{I_{tail}^2}} \tag{3.34}$$

tail current noise can dominated by either thermal noise in case of using degeneration resistor or shot noise. If shot noise dominates, which has density of;

$$i_{n,tail}=\sqrt{2qI_{tail}} \tag{3.35}$$

substituting (3.35) in (3.34) gives,

$$\sigma_t=\frac{i_{n,tail}}{2}\sqrt{\frac{R_LC_L}{I_{tail}^2}}=\sqrt{\frac{q.R_LC_L}{2.I_{tail}}} \tag{3.36}$$

Figure of merit, κ becomes (rms),

$$\kappa = \frac{\sigma_t}{\sqrt{T_d}} = \frac{\sqrt{\frac{q.R_L C_L}{2.I_{tail}}}}{\sqrt{\ln(2).R_L.C_L}} = \sqrt{\frac{1}{2.\ln(2)}}.\sqrt{\frac{q}{I_{tail}}} \cong 0.849.\sqrt{\frac{q}{I_{tail}}} \tag{3.37}$$

This is similar to (3.29), where κ was given by a smallest resolvable energy as a fraction of energy flow. In (3.37), the differential pair's ability to resolve time is characterized by the smallest resolvable unit of charge (q) as a fraction of the charge flow over time (I_{tail}).

If the tail current source is degenerated, then the thermal noise density of the degeneration resistor R_E should be used:

$$i_{n,tail} = \sqrt{\frac{4kT}{R_E}} \tag{3.38}$$

when (3.38) substituted in (3.34)

$$\sigma_t = \frac{i_{n,tail}}{2}\sqrt{\frac{R_L C_L}{I_{tail}^2}} = \sqrt{\frac{kT.R_L C_L}{R_E.I_{tail}^2}} \tag{3.39}$$

resulting κ for degenerated resistor case,

$$\kappa = \frac{\sigma_t}{\sqrt{T_d}} = \frac{\sqrt{\frac{kT.R_L C_L}{R_E.I_{tail}^2}}}{\sqrt{\ln(2).R_L.C_L}} = \sqrt{\frac{1}{\ln(2)}}.\sqrt{\frac{kT}{R_E.I_{tail}^2}} \cong 1.201.\sqrt{\frac{kT}{R_E.I_{tail}^2}} \tag{3.40}$$

In this case, (3.40) is similar to (3.29) in that the stage's ability to resolve time is characterized by the energy uncertainty (kT) as a fraction of the energy flow over time ($I_{tail}^2.R_E$) in the element that determines the current. Both (3.40) and (3.37) indicate that jitter is improved by increasing the DC power dissipation, similar to the result of (3.29) for the collector load resistors.

For lowest jitter contribution from tail current, the current source should be degenerated so thermal noise (not shot noise) is the limiting factor but this assumption holds for high degeneration resistor values (R_E), if lower R_E values mandated from voltage headroom problems, shot noise contribution could be preferable. Thus shot or thermal noise contributions have to be calculated according to implementation problems and should be carefully investigated.

3.3.2.3 Switching of Input Noise

This type of noise can be considered as sampling of the total input noise which are lumped to single source e_n, assuming all noise sources are white. Transfer function of a bipolar differential pair can be written as,

$$I_{out,diff} = I_{tail} \tanh\left(\frac{V_{in,diff}}{2V_T}\right) \tag{3.41}$$

where V_T=kT/q is the thermal voltage and tanh is the tangent hyperbolic function. The incremental gain, g_m, can be calculated as;

$$g_m = \frac{dI_{out,diff}}{dV_{in,diff}} = \frac{I_{tail}}{2V_T}\operatorname{sech}^2\left(\frac{V_{in,diff}}{2V_T}\right) \tag{3.42}$$

where sech is the hyperbolic secant. For input signals that are large compared to V_T, the gain to the output current is small. Thus the input voltage noise has little effect when the input signals are far apart. As the input signals cross over during switching, however, the gain rises. During this time, the input voltage noise produces a noise current which is integrated on the collector capacitors. Although the integration is "leaky" due to the discharge path through R_L, some of the integrated noise still remains when the collector voltages cross approximately T_d later. The strategy for analyzing this noise source is first to determine the standard deviation of the integrated noise current, and then determine how much of this influence remains when the output voltages cross.

These calculations can be found on [McNeill, J.A., 1994] and will not be depicted here. The resulting standard deviation of jitter;

$$\sigma_t = \frac{e_n}{2}\sqrt{\frac{C_L}{3.I_{tail}.V_T}} \tag{3.43}$$

Assuming the noise density to be dominated by thermal noise of the total base resistance r_{bT}, noise density e_n becomes,

$$e_n = \sqrt{4kTr_{bT}} \tag{3.44}$$

then substituting the base resistance noise density expression in (3.43) and V_T=kT/q results,

$$\sigma_t = \frac{e_n}{2}\sqrt{\frac{C_L}{3.I_{tail}.V_T}} = \sqrt{\frac{q.r_{bT}.C_L}{3.I_{tail}}} \tag{3.45}$$

normalized timing errors in rms fashion,

$$\kappa = \frac{\sigma_t}{\sqrt{T_d}} = \frac{\sqrt{\frac{q.r_{bT}}{3.I_{tail}}}}{\sqrt{\ln(2).R_L.C_L}} = \sqrt{\frac{1}{3.\ln(2)}}.\sqrt{\frac{q.r_{bT}}{I_{tail}R_L}} \cong 0.693.\sqrt{\frac{q.r_{bT}}{I_{tail}R_L}} \tag{3.46}$$

this expression is similar to tail current shot noise contribution but with a scaling factor that formed by total equivalent base resistance and the collector load resistance. The equivalent r_{bT} must include all wideband noise sources (emitter followers, etc.) going back to the V_{out} of the previous stage.

3.3.2.4 Conclusion

The effect of each independent noise source to the output of single delay stage can be combined in rms fashion thus allow to predict the jitter performance of the stages. Two different figure of merits has been defined one is the ratio of the jitter and stage delay, the second one is the same as the first one but in rms fashion and with square root relationship, κ, which is the ratio of the jitter standard deviation and square root of stage delay, in order to be able to have the chance of combining each noise source effects in rms fashion.

Above results are valid for the following assumptions;

-Stage delay is dominated by the differential pair delay, (emitter follower contribution is low enough, because its delay is directly depended on base-transit time, which is f_T).

-Differential pair delay is dominated by the single pole time constant, R_LC_L of the collector load. The magnitude of the differential signal is higher than thermal voltage, $V_T \approx 25mV$.

-All the noise sources are white and uncorrelated (thus superposition for calculations in the above analysis holds).

-The magnitude of the noise is small compared to the differential signal, where "first crossing approximation" is valid.

The calculated jitter values are dependent on circuit design parameters, also delay adjustment can be done by varying the design parameters, which are related to jitter. Thus it is convenient

define a figure of merit relating the delay adjustment circuit design parameters that affect the jitter performance of the circuit. Two different figures of merits have been defined according to [Weigandt, C., 1998] and [McNeill, J.A., 1994], which are the ratio of standard deviation of jitter and stage delay and variance of jitter and stage delay (more convenient form of second one is the ratio of the jitter standard deviation and square root of the stage delay).

According to the above results for κ, equations (3.29), (3.37), (3.40) and (3.46) repeated below, shows no dependency on load capacitance C_L, thus delay adjustment can be done with varying the load capacitance without sacrificing jitter performance.

Collector load resistor thermal noise contribution;

$$\kappa \cong 1.699.\sqrt{\frac{kT}{I_{tail}^2.R_L}} \tag{3.47}$$

Tail current shot and thermal noise contributions respectively,

$$\kappa \cong 0.849.\sqrt{\frac{q}{I_{tail}}}, \tag{3.48a}$$

$$\kappa \cong 1.201.\sqrt{\frac{kT}{R_E.I_{tail}^2}} \tag{3.48b}$$

Switching equivalent base resistance thermal noise contribution,

$$\kappa \cong 0.693.\sqrt{\frac{q.r_{bT}}{I_{tail}R_L}} \tag{3.49}$$

3.3.3 DLL Noise Consideritions

Previous section describes jitter calculation for a single delay stage. In practice, voltage controlled delay line incorporates numbers of delay stages in cascaded configuration and thus delay chain configuration has to be examined.

Interstage gain considerations determine the jitter performance of cascaded buffer stages as in VCDL. Weigandt had shown that a stage experiencing a gain of a_v, differential pair amplifies the input noise density to its output for CMOS differential pairs [Weigandt, C., 1998]. But also it well known that when a differential pair is fully switched, meaning input differential voltage is high enough (in bipolar stages $>V_T$ [McNeill, J.A., 1994]), experiences very low

gain thus, this contribution is very low. When stages shoots switching, during switching transient, gain increases thus, amplifies input noise to its output by exponentially growing function of gain for bipolar stages, reaches its peak value at balanced instant then begins to drop exponentially. Thus, higher gain range input noise contribution will be higher than predicted above calculations.

Weigandt again had shown that ideal buffer assumption is a good approximation for cascaded buffers [Weigandt, C. and Kim, B. and Gray, P. 1994]. Thus total VCDL output jitter variance, for number of N delay stages, can be written in terms of single buffer jitter variance;

$$\sigma^2_{VCDL} \cong N.\sigma^2_{ps} \tag{3.50}$$

where "ps" subscript denotes total jitter per stage, including all noise sources. This approximation will help us to determine total VCDL output jitter (thus phase noise), and also, each tap output jitter of the VCDL, which is important for multiphase clocking applications of DLL.

Noise Properties of Edge Combining Action

In case of frequency multiplication, output jitter/phase noise profile has to be calculated in order to predict the performance of the local oscillator. It is well known that ring oscillator based frequency synthesizer accumulates jitter in every cycle resulting poor phase noise performance, but VCDL based oscillators reset the jitter accumulation to zero in every cycle thus have better phase noise performance (Figure 3.16 [Chien, G., 2000]).

Phase noise is the random timing fluctuation of zero crossings in an oscillation period, thus a sinusoidal wave including discrete-time timing errors X(t), can be written as,

$$S(t) = A(t).\cos(2\pi f_c(t - X(t))) \tag{3.51}$$

where A(t) is the amplitude, f_c is the carrier frequency in Hz. (3.51) can be re-written by trigonometric manipulations,

$$S(t) = A(t).\cos(2\pi f_c t).\cos(2\pi f_c X(t)) + A(t).\sin(2\pi f_c t).\sin(2\pi f_c X(t)) \tag{3.52}$$

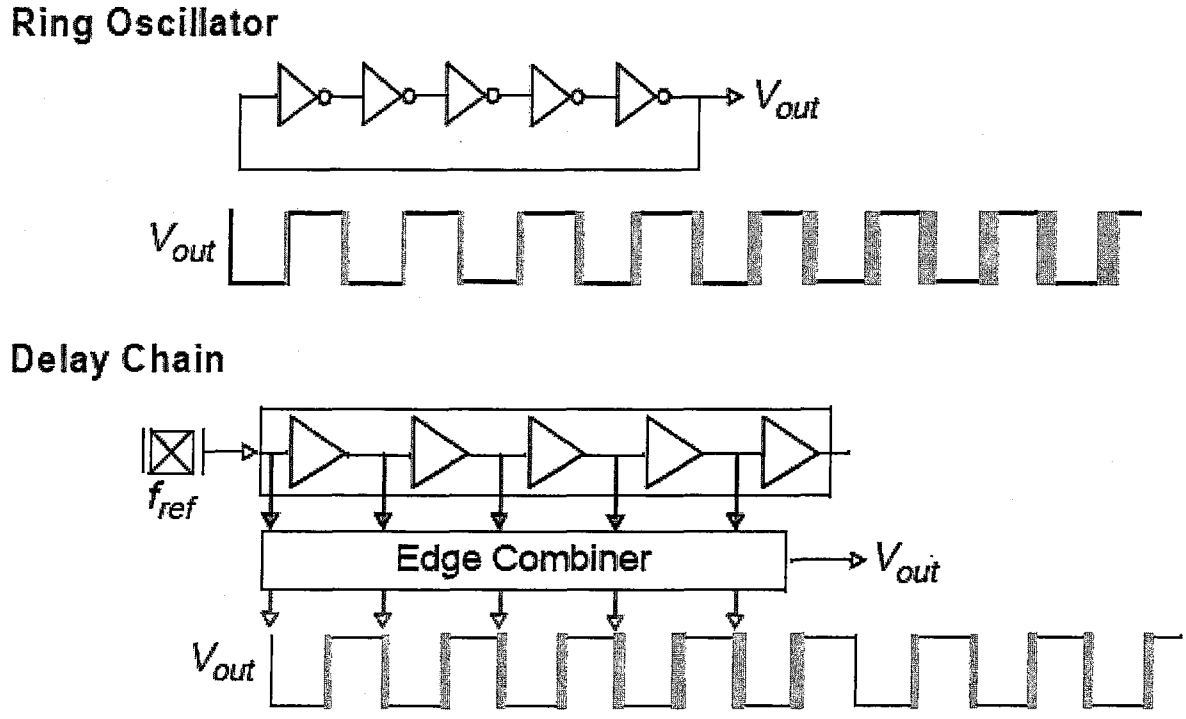


Figure 3.16 Timing jitter accumulation for Ring Oscillator VCO vs. Delay Chain

assuming the random timing error is much smaller than the oscillation period, X(t) can be approximated with a discrete-time impulse function,

$$X(t) \equiv X(n\bar{T}) \qquad n \in I, \tag{3.53}$$

where the $\bar{T}$ is the period of the carrier frequency ($1/f_c$), and approximating

$$\cos(2\pi f_c X(n\bar{T})) \cong 1 \text{ and } \sin(2\pi f_c X(n\bar{T})) \cong 2\pi f_c X(n\bar{T}) \tag{3.54}$$

Equation (3.52) becomes,

$$S(t) \cong A(t).\cos(2\pi f_c t) + A(t).[2\pi f_c X(n\bar{T})]\sin(2\pi f_c t) \tag{3.55}$$

where the first term is the carrier and the second term is the noise power. The phase noise term is a low frequency noise component modulated up to the carrier frequency by $\sin(2\pi f_c t)$.

Phase noise can be defined as the ratio of the noise power and carrier power, thus specified in dBc/Hz. If the oscillation amplitude is constant, A, which is the case for DLL based synthesizer.

$$\frac{\text{NoisePower}}{\text{CarrierPower}} = \frac{\frac{1}{2}.(A.2\pi f_c)^2.\left[S_{X(n\bar{T})}(f)\right]}{\frac{1}{2}.A^2} = (2\pi f_c)^2.\left[S_{X(n\bar{T})}(f)\right] \tag{3.56}$$

where the carrier signal is a deterministic signal with the power of $A^2/2$ but in order to find the noise power, the power spectral density of the of the random process, $X(n\bar{T})$ has to be estimated.

If we define a random variable "a_{ij}" where index i indicates the specific delay stage, and index j specifies the number of delay chain cycles. The second term is needed because DLL accumulates the jitter within one cycle but other cycles are not affected. If the random timing errors of each delay stage independent and have zero mean and Gaussian distributed with variance σ^2,

$$E[a_{ij}] = 0,\ E[a_{ij}^2]=\sigma^2. \tag{3.57}$$

For five stage example, $1\le i\le 5$, $X(0.\bar{T}) = 0$, $X(1.\bar{T}) = a_{11}, X(2.\bar{T}) = a_{11} + a_{21}$ ..., which is (Figure3.17),

$$X(n\bar{T}) = \sum_{i=1}^{n} a_{i1} \quad \text{for } n<5 \tag{3.58}$$

second oscillation cycle begins with $X(5.\bar{T}) = 0$, $X(6.\bar{T}) = a_{12}$, $X(7.\bar{T}) = a_{12} + a_{22}$ thus in general,

$$X(n\bar{T}, j) = \sum_{i=1}^{n-(j-1).N} a_{ij} \tag{3.59}$$

PSD of the timing error random process is the Fourier transform of the autocorrelation function. Autocorrelation function is,

$$R_{XX}(\tau) = E\left[X(n\bar{T})\cdot X(n\bar{T}-\tau)\right] \tag{3.60}$$

for five delay stage example, N=5 and for τ=0, the autocorrelation equals the variance of the random process,

$$R_{XX}(\tau) = E\left[X(n\bar{T})\cdot X(n\bar{T})\right]\frac{1}{5}.(0+\sigma^2+2\sigma^2+3\sigma^2+4\sigma^2) = 2.\sigma^2 \tag{3.61}$$

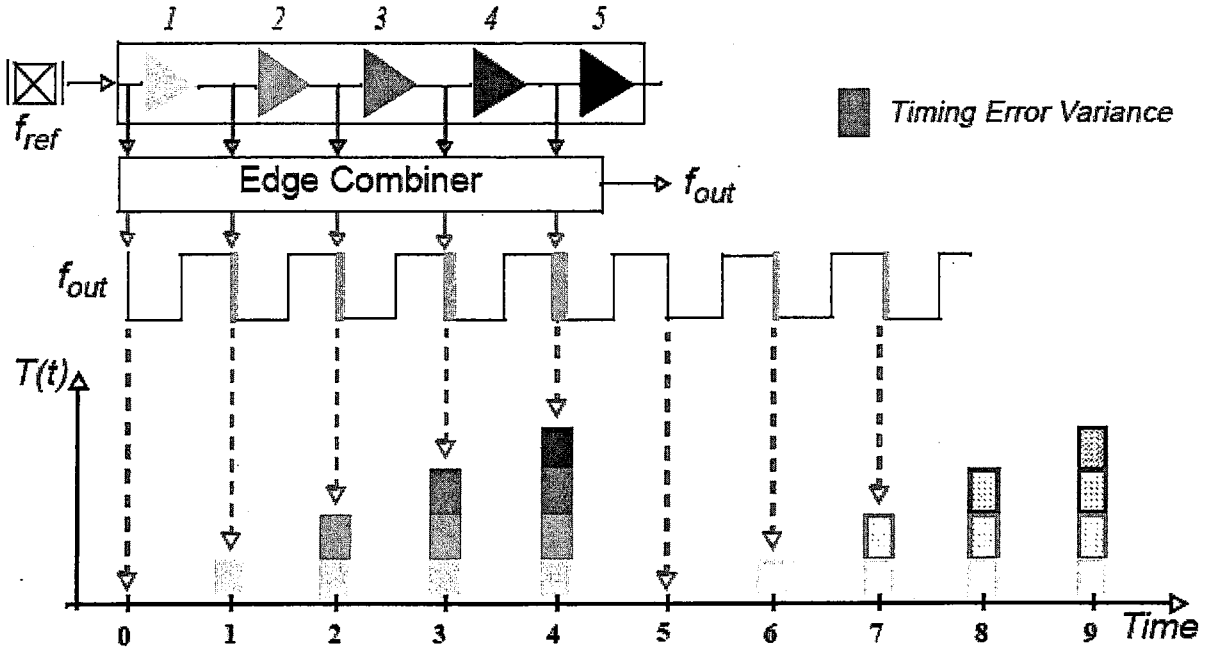


Figure 3.17 Timing jitter accumulation for 5-stage example

for τ=1, the autocorrelation function is the expected value of the random process multiplied by a shifted version itself and summed,

$$R_{XX}(\tau) = E\left[X(n\bar{T}) \cdot X(n\bar{T}-1)\right] = \frac{1}{5}.(0+\sigma^2+2\sigma^2+3\sigma^2+0^2) = 1.2\sigma^2 \tag{3.62}$$

for τ>1, correlated ones are considered. The uncorrelated overlapping ones of first cycle and second cycle is zero thus for τ=2,

$$R_{XX}(\tau) = E\left[X(n\bar{T}) \cdot X(n\bar{T}-2)\right] = \frac{1}{5}.(0+\sigma^2+2\sigma^2+0+0^2) = 0.6\sigma^2 \tag{3.63}$$

general expression becomes,

$$R_{XX}(\tau) = \frac{1}{N}\sum_{k=-(N-2)}^{N-2}\left[\delta(\tau-k)\cdot\sum_{u=1}^{N-|\tau|-1} u.\sigma^2\right] \tag{3.64}$$

PSD can be written as Fourier transform of the autocorrelation function, which is,

$$S_X(f) = \sum_{n=-\infty}^{\infty} R_{XX}(n).e^{-jfn} \tag{3.65}$$

Equations (3.64) and (3.65) gives the power spectral density. For five stage example it becomes,

$$S_X(f) = \left[2 + \frac{12}{5}\cos(f) + \frac{6}{5}\cos(2f) + \frac{2}{5}\cos(3f)\right].\sigma^2 \tag{3.66}$$

and for six delay stage PSD becomes,

$$S_X(f) = \left[2.5 + \frac{20}{6}\cos(f) + \frac{12}{6}\cos(2f) + \frac{6}{6}\cos(3f) + \frac{2}{6}\cos(4f)\right].\sigma^2 \tag{3.67}$$

where σ^2 is the variance of the jitter per stage. (3.66) and (3.67) imply that at low frequencies, cosine terms are equal to one and PSD has profile constant, as the frequency increases PSD falls further. Keeping delay stage jitter at lower values directly lowers the phase noise.

Noise Properties of Delay Stage Mismatch

It is also important to calculate delay stage mismatches, which is statistically varies with the matching properties of the elements used in a stage defined by the process parameters, and is problematic while DLL is used as frequency multiplier or multiphase clock source. In locked condition delay stage mismatches result spurious tones at reference clock frequency away from the carrier in frequency multiplication and ADC output while mismatched multiphase clock signals are used.

van de Beek had shown that, stochastic mismatches between the delay cells causes skew of the intermediate clock phases [van de Beek, R., 2002]. This phenomenon manifests itself as systematic jitter on the high frequency clock in case of frequency multiplication. Which is,

$$\sigma_m^2 \cong T_s^2 \cdot \frac{m(M-m)}{M^3}\sigma_{en}^2 \tag{3.68}$$

where σ_m^2 is the variance of mismatch caused skew, T_s sampling period, m is the m^{th} tap of VCDL, M is the number of delay stage and σ_{en}^2 is the variance of the mismatch and dependent on control voltage. According to formulation, maximum value of σ_m^2 is at the halfway of the VCDL where m=M/2. Thus maximum standard deviation of skew is,

$$\sigma_{\frac{1}{2}M} \cong \sigma_{en}\frac{T_s}{2\sqrt{M}} \tag{3.69}$$

this result is predictable because the loop controls the VCDL such that the time error at its output is zero, while the error at the input of the VCDL is zero. The highest timing

uncertainty will be in the middle of the VCDL, where the distance to these clean points is highest.

This result should not be confused with VCDL jitter that arises from the time-varying noise sources. Element mismatches in an IC are defined with statistically, thus when one IC is produced, the mismatch affect was deterministic and that result in a DLL as constant skew values, thus in various DLL applications, the error is spurious tones. But above result can be used to estimate the control voltage noise consequences, which can be caused by the coupling of other noise sources in implementation practice because of control voltage dependency.

4 A 4GHz SiGe HBT DLL DESIGN

The goal of this research is to implement named a core DLL working on 4GHz clock signal. Design procedure also captures the possible different applications of DLL, which are skew cancellation, multiphase clocking and frequency multiplication. Thus, final version of core DLL could be a little tailored for a dedicated application using different kind of specifications such as power consumption, silicon area, noise behavior and the loop dynamics.

After designing core DLL, some researches have been made in order to exploit benefits of DLL. Two different edge combiner circuits have been designed in order to take a chance of comparing them for their phase noise performances producing up to 30GHz clock signals. These works are still in progress, which prevent finalizing the top-level considerations for a test chip. Also circuit design techniques for HBT devices had been investigated.

DLL design had been made using 3.3V 0.35μm SiGe HBT BiCMOS process parameters which has two SiGe modules besides CMOS core modules and passive elements,

-high speed SiGe HBT module ($f_T \approx 70$GHz and $BV_{CEO} \approx 2.7$V)

-high voltage SiGe HBT module ($f_T \approx 30$GHz and $BV_{CEO} \approx 5.5$V)

Both of the modules have been used in the design of DLL for different kind of purposes.

Performance estimation of the DLL, especially noise behavior, has been a problem because of increased simulation time thus estimations had been made based on the techniques described on previous chapter. Design is verified for different process corners for used devices and temperature range of -20°C to 130°C, in order to be sure of proper operation of the DLL. Basic circuit simulator was Spectre and during performance estimation SpectreRF has been used.

Each transistors biasing conditions in the design was determined by primarily considering the f_T-I_C and β-I_C characteristics and may vary for kind of purposes. Voltage swings and biasing conditions of each circuit may also differ from each other.

The core DLL is working on 4GHz (T_{ref}=250ps) clock signal and implemented Type-I because of the higher operation frequency and some application problems. Each building block will be presented respectively.

4.1 Phase/Frequency Detector

Tri-state phase/frequency detector is chosen here as a phase detector because of its far superior capture range and tracking behavior and also its ease in implementation conjunction with a charge pump and loop filter. Also, DLL will be used with clock signals, not for data applications, so there is no need for flywheel capability. Block diagram of the phase/frequency detector (PFD) is shown in Figure 4.1.

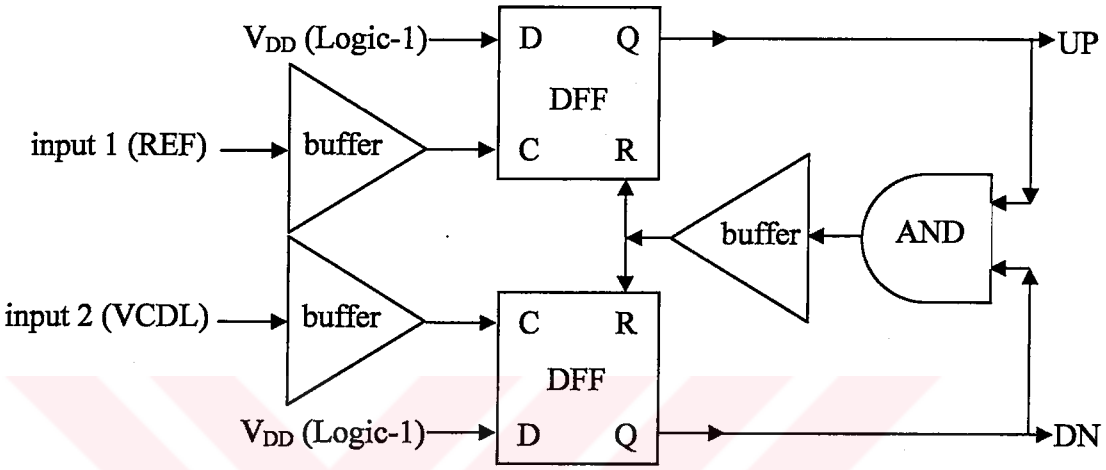


Figure 4.1 Phase/frequency detector block diagram.

Flip-flops, seen in the block diagram, are the major component of the PFD that mostly determine the performance of the PFD. DFFs, input buffers and AND gate are designed to work at higher frequencies up to 6GHz for all process corners and temperature variations in order to be able to operate DLL at those frequencies. Input buffers take place in the diagram in order to supply the clock signals to DFFs at desired condition, which are common mode level and voltage swing of the input signals. Buffers should experience same amount of delay on either reference signal and VCDL output signal, if not DLL will be locked with a static phase error. As mentioned in chapter 2.1.2 it is important to prevent static phase error that could occur because of reset and data delay of the flip-flops and so AND gate delay. In the block diagram there is no extra buffer in reset path, because AND gate experiences more delay than flip-flops that prevents static phase error.

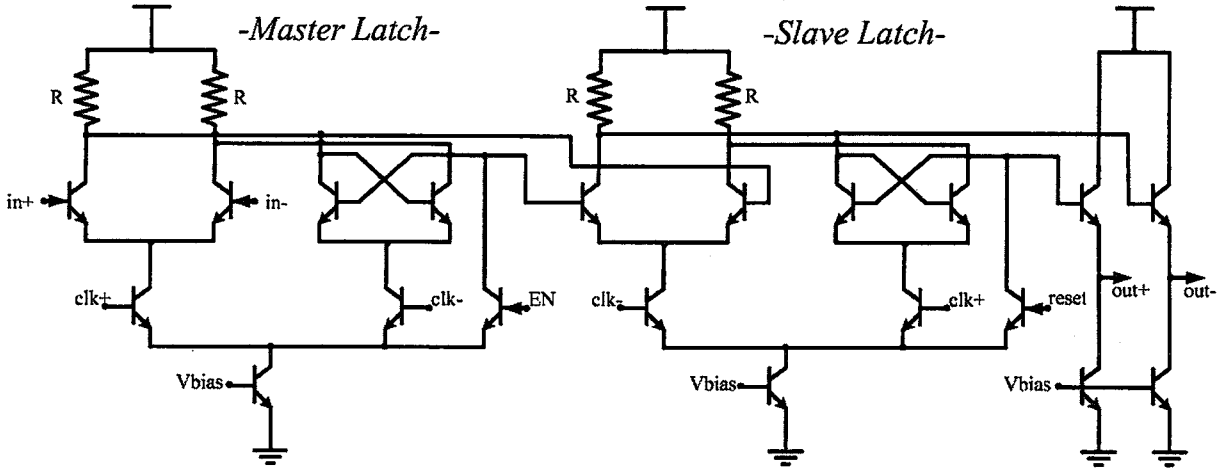


Figure 4.2 Master-slave DFF.

Negative edge triggered differential DFFs constructed with two latches with master-slave configuration, a well known topology (Figure 4.2). If "clk+" is high, first stage is at the preamplifier state while the second latches. When "clk–" goes high, first stage latches and produces the output because second is transparent at the moment. Voltage swings is chosen $200mV_{pp}$ (4.1) that is far above the $4.V_T$ (≈105mV) value, which is necessary for complete switching of the tail current. In bipolar stages, this amount of voltage swing is advantageous because it prevents the input stage transistors of the second stage to go to the saturation for all cases without using any level converter such as emitter followers (EF). At the output, EFs are used in order to increase the driving capability of the DFF. The buffers experiences some delay of course and is taken into account while managing the reset path delay thus AND gate delay is arranged to minimize the dead-zone.

$$\text{VoltageSwing} = V_{SW}(V_{pp}) = I_{tail} \times R_{load} \tag{4.1}$$

Clock signal common mode voltage is limited by the saturation of the tail current supply transistor and stacked transistors. Thus common mode signal is chosen higher than 1.3V, which is provided by input buffers. DC biasing of the stage is accomplished by keeping in mind that the bandwidth considerations of the stage and also switching speed of the each stage thus, differential rise/fall times (while in transparent mode), which result higher current levels and reduced load resistors which limit the bandwidth of the stage (I_{tail}=2mA, R_{load}=200Ω). Higher collector currents result higher base current that has effect on preceding stage thus β-I_C characteristics of the devices are also taken into account where necessary.

In both latches, stacked transistors prevent and breakdown with appropriate voltage headroom managing, but emitter followers could suffer from breakdown phenomenon of high speed

HBT modules, at the output stage. Thus, biasing conditions of such stages are carefully arranged in order to prevent any unwanted situation. For example, under V_{DD}=3.3V condition and leaving 700mV to the collector of the tail current results V_{CE}=2.6V of the emitter follower transistor. This V_{CE} value is at the limit of the given typical value for the B_{VCEO}. Thus, V_{CE} voltage is reduced by leaving more voltage headroom to the current sources. Also biasing conditions and device areas of EFs especially cascaded ones, which is the case for input buffers (Figure 4.3), and the other digital circuits, have been determined considering the loading effects, ringing phenomenon and bandwidth limits. Further design strategies could be found on [Rein, H. and Moller, M., 1996].

The type and the area of the current source transistors had been chosen according to seen output impedances at the operating frequency and collector current densities. This yield a general approach of using high voltage SiGe HBT modules as tail current transistors with varying area for different circuits MOS transistors are not adequate for 4GHz operation and lower overdrive voltages at those higher current levels because of lower output impedance and requirement of large areas in order to reduce overdrive voltages.

Reset input of the DFF is placed parallel to the second stage latching transistors. If reset signal is high, the tail current will be directed to the load resistor determining positive output, thus producing logic low and asynchronous reset action is achieved. Reset signal voltage swing has to be large enough in order to take action, independent of the clock input levels. In first stage another reset transistor have placed, but this input is used as DC enable input to configure the DLL loop (for example start-up condition) by disabling the phase error signal, and thus leaving the control voltage constant which will be explained later.

Input buffers are needed in order to drive flip-flops properly. It should be noted that reference signal is applied to both the VCDL input and the PFD reference input, which may cause driving problems. Also large interconnects in the layout for both input signals could reduce the voltage swing and thus rise/fall times of the signals. Large or unbalanced interconnects for the reference and VCDL output signal could also result different amount of delays that directly affects the static phase error, and should be minimized by proper layout techniques.

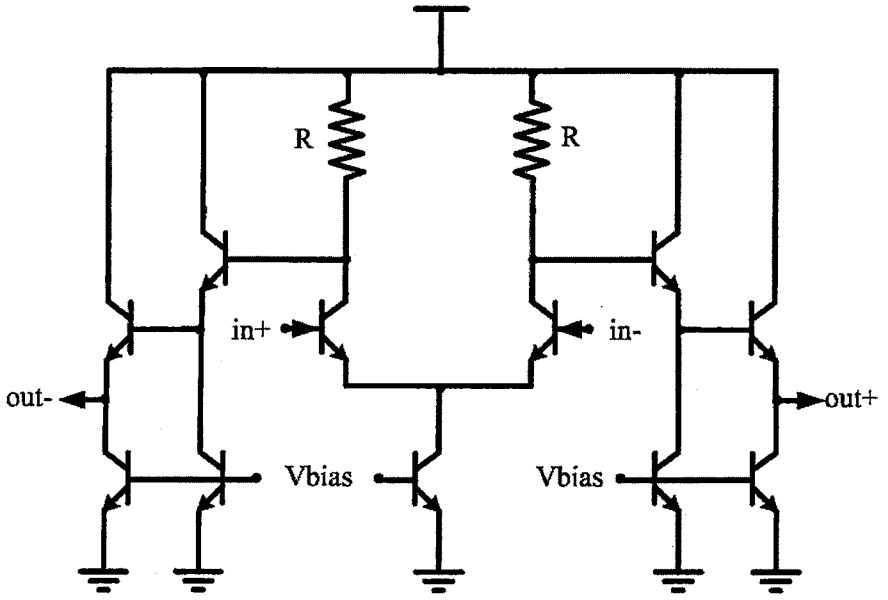


Figure 4.3 Input buffer cirtcuit schematic.

Setup and hold time of DFF is out of interest because DC inputs will be applied to their data inputs in PFD configuration, but DFF experiences no setup time (sub picoseconds) and a little hold time, dominated by latch pair transistors recover time. DFF can operate up to 6GHz clock input signals safely.

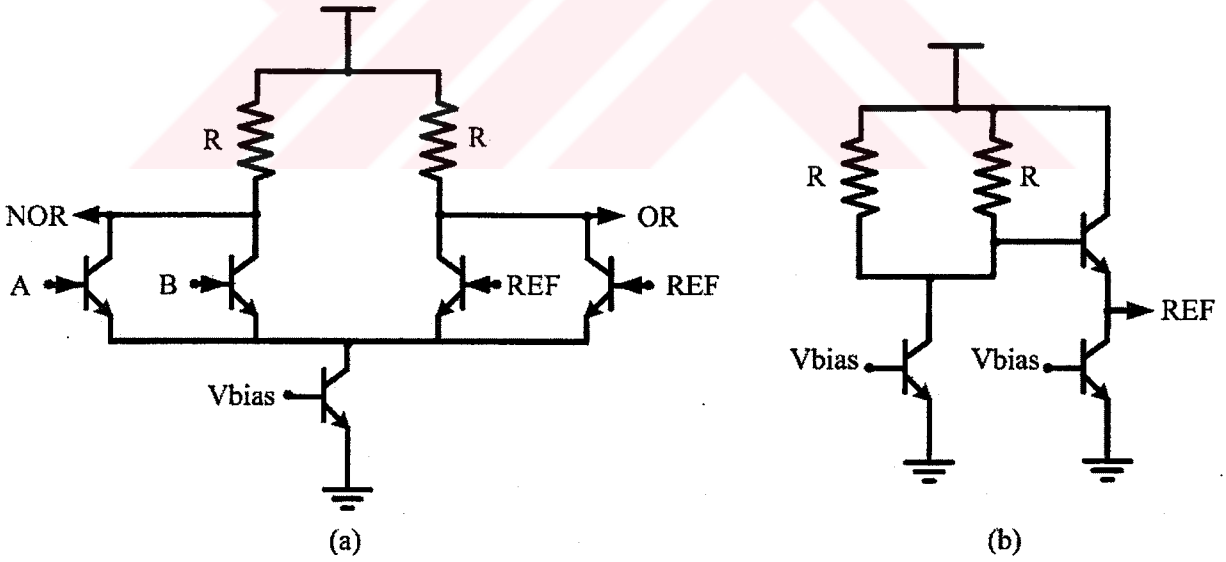


Figure 4.4 (a) OR gate schematic and (b) its DC reference generator

In order to built up PFD, AND gate function, which is impossible to implement in ECL logic family, has charged to OR gate. Logic function of AND gate is

$$Y = A.B \tag{4.2}$$

and could be rewritten as;

$$Y = A.B = (A`+B`)` \quad (4.3)$$

This equation suggests that an NOR gate with negative inputs results AND gate function. An AND gate is designed in CML logic which could work at higher frequencies. But increased power consumption of CML gate and reasonable OR gate performance make us to choose ECL OR gate implementation, seen in the Figure 4.4a. There is no need for an additional inverter stage for negative inputs because differential outputs of flip-flops provides negative inputs. This block will be called AND gate because of it outputs AND gate function although built up with an OR gate.

A and B inputs are compared with a DC reference which is the common mode level of the input signals and generated by a replica of the DFF output stage which produce the data signal (Figure 4.4b). Same tail current copied to same resistor value and a level shifter (EF) produces the desired DC reference value. DC reference can be implemented in several ways, a resistor voltage divider comes to mind first, but its PVT variations sensitivity and supply noise immunity is very low compared to chosen reference generator, which has a low impedance output node make them insensitive to supply noise and also it tracks the changes of the common mode variations of DFF output that can result of the tail current and resistor value variations. Also a low pass filter with a very low cutoff frequency can be used to sense the DC level of the inputs but requires high capacitor values that would waste silicon area.

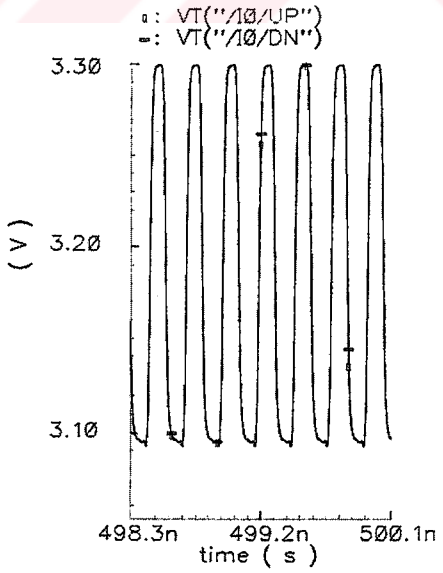


Figure 4.5 Simulation example for up and down signals in locked condition

Both circuits' biasing conditions have been arranged according to explanation made on flip-flop design procedure. Voltage swing of $200mV_{pp}$ had been chosen. In order to have higher

reset signal voltage swing higher than clock signals' in flip-flops and manage the reset path delay, as explained before, another buffer stage is used which has a $500mV_{pp}$ voltage swing and delay of lower than 70ps (Figure 4.5). Higher amount of reset delay will decrease the capture range of the PFD and could result serious operation problems that has to be avoided.

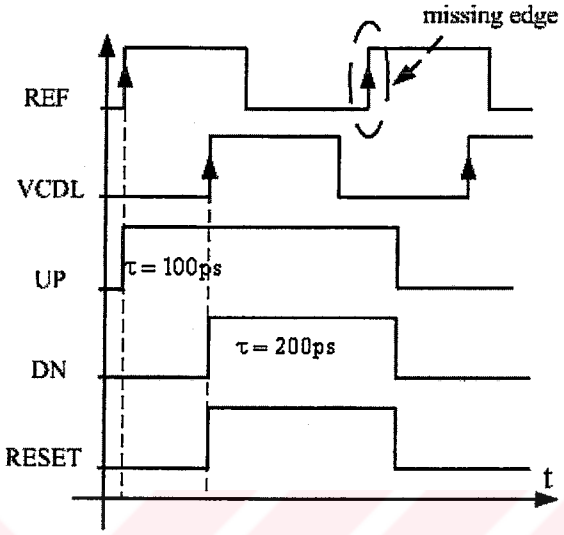


Figure 4.6 Nonideal behavior of PFD caused by increased reset path delay

Consider a phase difference between reference and VCDL output of 100ps and reference leading VCDL and reset path delay of more than 150ps say it 200ps (for positive edge triggered PFD, Figure 4.6). Knowing that the reference period is 250ps, after 100ps of UP signal, DN signal will go high and AND gate inputs will be both high thus allows reset signal to rise. But reset signal will appear at the inputs of the flip-flops after 200ps thus, total pulse width for UP signal will be 100ps+200ps=300ps which means that, next reference signal edge will be missed. The missing edge corresponds to comparison at half rate that cause input signal dependent change in the DLL loop dynamics. This could be done on purpose in order to reduce comparison frequency and manipulate the loop dynamics but should be carefully managed.

Figure 4.7 shows simulated PFD characteristics. Up and downs signal pulse time had been calculated and extracted with each other in order to determine the charge injection time to the loop filter of the charge pump which accepts UP and DN inputs. As can be seen in the figure, PFD experiences zero dead-zone.

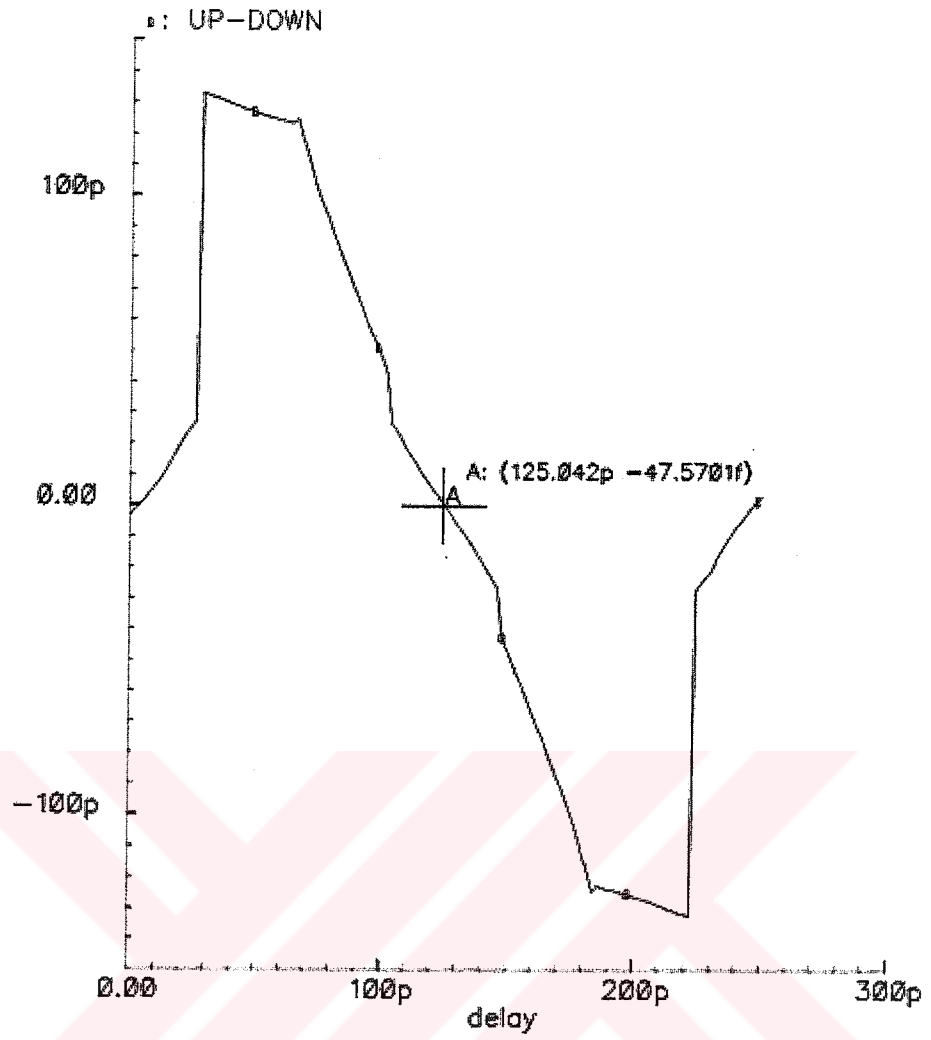


Figure 4.7 Phase/frequency detector characteristic experiencing zero dead-zone.

4.2 Charge Pump and Loop Filter

The problems could result from the charge-pumps have already been discussed in chapter 2.2. Using two separate current sources in order to add/remove charges from the loop filter capacitance, current mismatch of the sources would result static phase error under locked condition of the DLL. Theoretically, current mismatch does not cause problem when the loop is locked if there is no up or down signals from the PFD. But in practice, additional reset path delay that is introduced in order to eliminate dead-zone in PFDs, would cause current sources remain on all the time and in case of the current mismatch DLL suffers from this error.

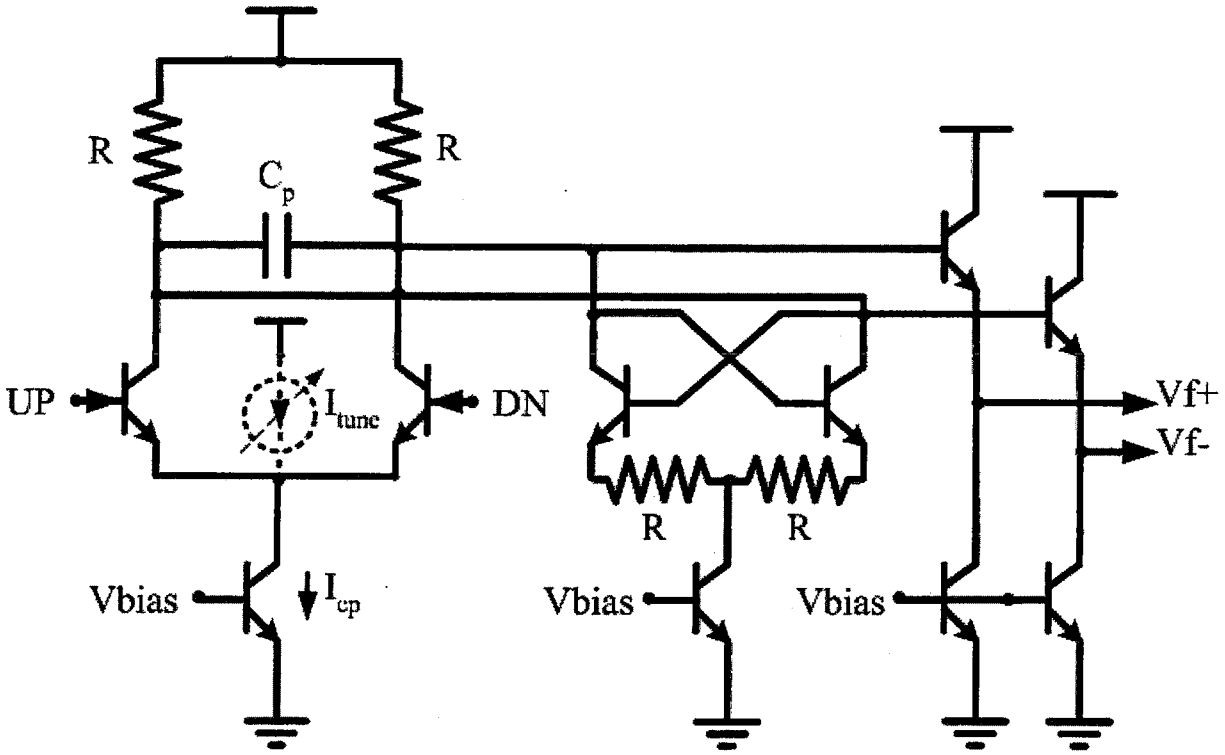


Figure 4.8 Charge pump schematic

In order to prevent any current mismatch, only one current source has been used in the charge pump (Figure 4.8). UP and DN signals' positive ones from the PFD, direct the tail current to one side and give raise to corresponding node voltage thus charge pump produces differential control voltage. Single-ended UP and DN signals can seem to be problematic, but it is verified with the simulations that, current mismatch in two tail current sources occupied in differential implementation is more problematic for the DLL.

Load resistors (R) are used to maintain common mode level and gain of the circuit. Also resistor values are chosen with higher values that degrade the bandwidth of the stages. This feature is useful, reducing high frequency ripple on the control voltage can cause from feedthrough or coupling of the 4GHz high speed signals around the stage. A cross-coupled pair degenerated by resistors (R) is a negative impedance converter (NIC) generates negative AC resistance, which is used to cancel the effects of load resistors. Mismatch of the load and degeneration resistors will result a parasitic resistance parallel to the loop filter capacitance and can deviate the pole from zero. Also AC base currents of cross coupled pair can have effect on mismatch resistor value thus tail current has to be lowered enough for ignorable AC base currents. The common mode voltage level of the differential signal produced on the capacitor nodes are also affected by the NIC tail current thus is taken into account.

Capacitor value is chosen to be $C_p \approx 275pF$ and the charge pump current is $I_{cp}=1mA$. Capacitor value and charge pump current are only two adjustable parameters determining DLL loop dynamics. Thus a tuning current source is placed in the circuit in order to being able to adjust the charge pump current and thus the loop bandwidth of the DLL for testing purposes. Thus combined PFD and charge pump gain is;

$$K_{PD\_CP} = \frac{I_{cp}}{2\pi} \tag{4.4}$$

The capacitor is implemented with high capacity stack capacitor that is built up with poly-poly section and well capacitor allowing high level integration but some parasitic resistances could occur cause of the well thus should be taken into account for the sake the loop dynamic analysis.

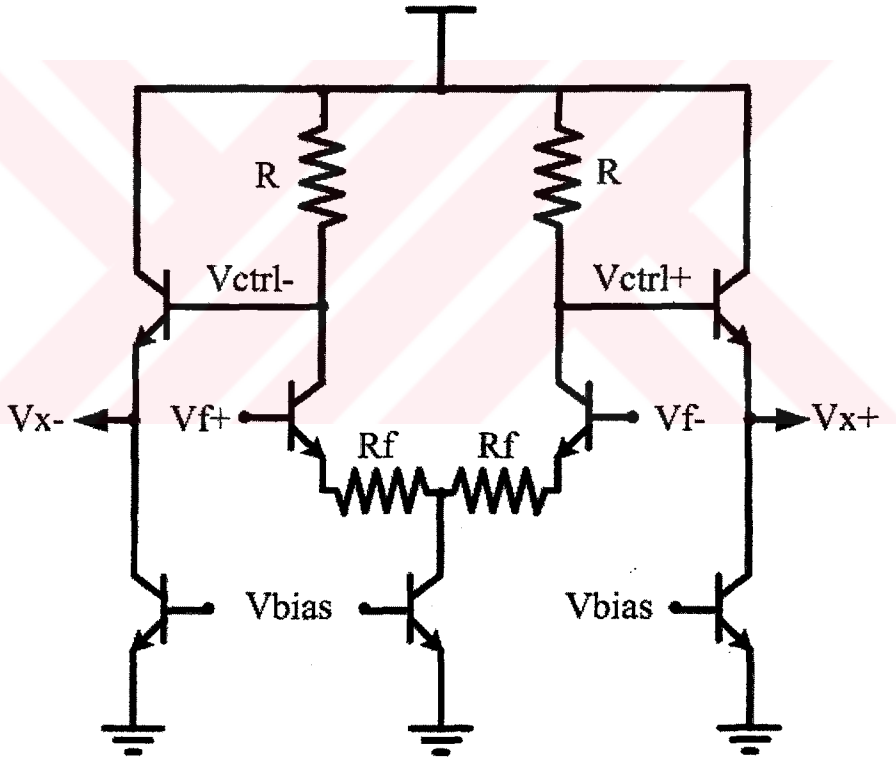


Figure 4.9 Charge Pump output stage

Differential control signal at the capacitor nodes has to be converted to single-ended and level shifted, because of the delay stage demands of the VCDL. Thus control signal is buffered with emitter followers and a differential pair is used to produce proper control voltage for the VCDL. Charge pump output stage is shown in Figure 4.9. The stage is linearized around the common mode voltage level and peak value limits of the charge pump output voltage (V_f+,V_f-) with the degeneration resistors (R_f). Voltage gain of the stage can be written as

$$K_v = \frac{R}{r_e + R_f} \tag{4.5}$$

The gain of the stage is chosen a little above the unity. In case of having higher gains, the amount should be added to combined phase detector and charge pump gain. Single-ended control signal that is applied to VCDL, $V_{ctrl}+$, is between 1.6V-3.3V determined by the delay stage linear control range. Level shifted version of the differential control voltage, V_x+ and V_x- are used for DC biasing purposes of the VCDL, which will be explained in next section.

Start-up conditions for classical charge-pumps could be problematic because initial charge or voltage level of the capacitor can drive following circuits (VCOs, VCDLs) improper operation range. This can put DLLs or PLLs to an undefined operation range and loops can never be able to recover and thus be locked. But proposed design does not suffer from possible improper start-up condition. But some modifications have been done for testing purposes which will be explained chapter 5.

Figure 4.10 shows control voltage variations while DLL loop is in progress to be locked with additional voltage noise added to control voltage ($20mV_{pp}$), in order to determine the consequences of the control voltage noise [chapter 3].

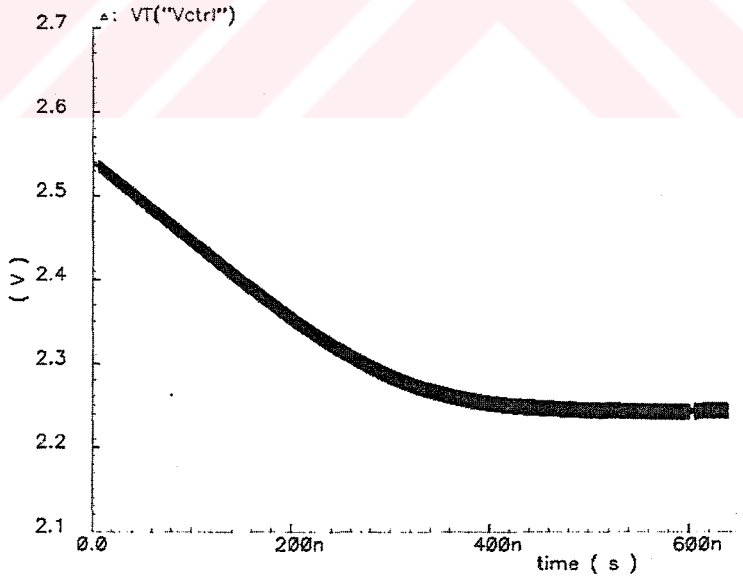


Figure 4.10 Control voltage versus simulation time

4.3 Voltage Controlled Delay Line

The most important part of the DLL design is the VCDL. There are many goals in VCDL design such as power consumption, VCDL gain, linear delay control range, low phase noise

etc. All these requirements have trade-offs with one and another thus make the design challenging. Application area of the DLL can also tighten some of the specifications while loosen the others. Also some requirements depicted before that VCDL should have, independent of the application areas, like monotonicity and variable delay range that determines the capture range of the DLL, which has to be equal to at least one period the reference signal frequency. Also in case of multiphase clocking and frequency multiplication applications each delay stage those built up VCDL, has to experience equal phase shift for a corresponding control signal.

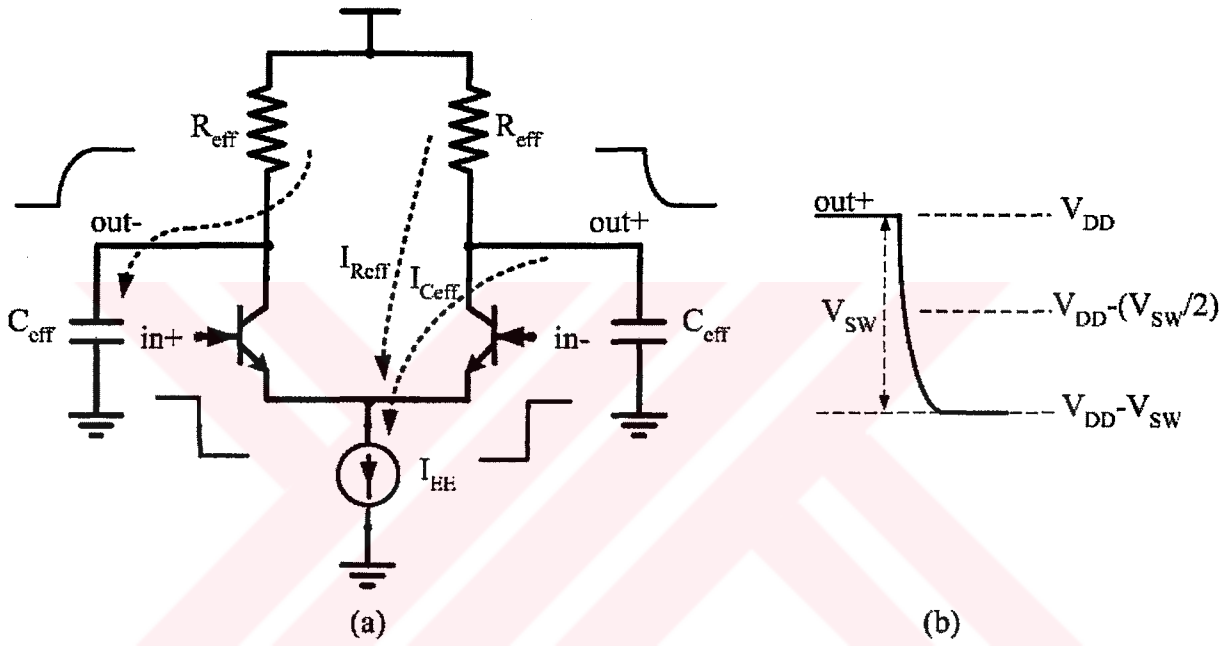


Figure 4.11 Emitter-Coupled stage dynamic behavior

4.3.1 Delay Stage Design

VCDL design relies on basic delay stage, whose delay can be adjusted different ways as explained in section 2.4. It is convenient to repeat that delay adjustment relies on varying the time constant output node of the stage that is;

$$\tau \approx R_{eff} \times C_{eff} \tag{4.6}$$

Most of the delay stage designs in the literature are based on adjusting the R_{eff} and rarely C_{eff}, whether for ring oscillator VCOs or VCDLs. Considering an emitter-coupled stage as shown in Figure 4.11, delay of the stage can be written in form of capacitance charge and discharge time equations.

When input goes high (in–) relevant transistor turns on and the other turns of thus output signal (out+) go low by discharging load capacitor with some the tail current (I_{Ceff}). When the out+ goes low further, some current starts to flow on the load resistor (I_{Reff}). Thus tail current can be written in form of two flowing currents;

$$I_{EE} = I_{Reff} + I_{Ceff} = \frac{V_{DD} - V_{out+}}{R_{eff}} + C_{eff}\frac{dV_{out+}}{dt} \tag{4.7}$$

and rearranging the above equation we get;

$$dt = \frac{C_{eff}}{I_{EE} - \frac{(V_{DD} - V_{out+})}{R_{eff}}} dV_{out+} \tag{4.8}$$

which allows to compute the time spend on two voltage levels. Rise/fall times can be calculated by proper definition of the ranges of the integral of the equation (4.8), seen in the Figure 4.11b. The stage delay can be defined as the times spend on the arrival to the midpoint of the voltage swing from the peak level. Keeping in mind that voltage swing V_{SW},

$$V_{SW} = I_{EE} \times R_{eff} \tag{4.9}$$

thus integrating equation 4.8 with the range of delay definition;

$$T_{dps+} = \int_{\left(V_{DD}-\frac{V_{sw}}{2}\right)}^{V_{DD}} \frac{C_{eff}}{I_{EE} - \frac{(V_{DD} - V_{out+})}{R_{eff}}} dV_{out+} \tag{4.10}$$

solving above equation results;

$$T_{dps+} = R_{eff}.C_{eff}.\ln\left(V_{SW} - V_{DD} + V_{out+}\right)_{\left(V_{DD}-\frac{V_{sw}}{2}\right)}^{V_{DD}} = R_{eff}.C_{eff}.\ln\left(\frac{V_{SW}}{V_{SW} - \frac{V_{SW}}{2}}\right)$$

$$T_{dps+} = \ln(2).R_{eff}.C_{eff}. \tag{4.11}$$

thus delay per stage can be calculated according to equation (4.11) and delay adjusting for a stage has to be done according to above result. Also equality of current flowing from load resistor to capacitor can be written for "out–" node which is;

$$\frac{V_{DD}-V_{out+}}{R_{eff}}=C_{eff}\frac{dV_{out+}}{dt} \tag{4.12}$$

arranging this equation for time delay results as;

$$T_{dps-}=\int_{\left(V_{DD}-\frac{V_{sw}}{2}\right)}^{V_{DD}-V_{sw}}\frac{C_{eff}}{\frac{(V_{DD}-V_{out-})}{R_{eff}}}dV_{out-} \tag{4.13}$$

and solving delay for negative edge results;

$$T_{dps-}=\ln(2).R_{eff}.C_{eff}. \tag{4.14}$$

If the stage delay is defined according to the signal crossing of the midpoint of voltage swing (or common mode voltage level), negative and positive edge crossings are equal as expected which can be seen in equations (4.11) and (4.14). Thus delay per stage, T_{dps}, is defined according to above result. It should be noted that if we consider rise and fall times, equality can be arranged with proper choice for load resistors and tail currents. Above results are valid for CMOS implementation of the stage as expected (ignorable switching delay can be defined as $t_d=\tau_T.(r`_b/R_L)+r`_bC_{jc}$ where τ_T is transit time, C_{jc} is the collector-base capacitance, $r`_b$ is a silicon resistor).

Delay stages can be designed to adjust the load resistors or load capacitors as mentioned before. Above results suggest that stage delay does not depend on tail current. But adjusting load resistors could result changing voltage swing, which is serious problem while driving the following stage and its operation. Thus in case of manipulating load resistor for delay adjusting action, tail current also has to be changed in the opposite direction in order to keep the voltage swing constant, which can be seen in equation (4.9). This requires additional feedback circuits which has to keep output voltage swing constant, by sensing the resistor value change and adjusting the tail current, those called "replica feedback bias" circuits developed by Maneatis. The bandwidth of the bias generator has to be set equal to the operating frequency if the delay stages so that the bias generator can track all supply and substrate voltage disturbances at frequencies that can affect the DLL. But in this work, delay stages have to operate at 4GHz clock frequency and likely at more than that. Thus it is hard to implement a feedback system that has a bandwidth of interested operating frequency range. A lower bandwidth feedback system can be useful but the advantages of that kind of system

vanishes and also some stability problems can arise which has to be avoided for the sake of the high frequency DLL.

It is almost impossible that the use of 0.35μm technology MOS transistors in the high frequency operating path, which is differential pair. Variable load resistors can be implemented as PMOS triod loads that have linear control range with HBT differential pair. But improper high frequency characteristics of the available pnp transistors in the technology, give only a chance of using npn's at 4GHz and above.

The problems mentioned above give only the chance of using capacitive tuning solution for the delay stages. Capacitive tuning can be accomplished with well known variable capacitors, named varactors. In this case, delay adjustment can be done with the controlling the variable capacitors, which is shown in the Figure 4.12a and PMOS varactor example is shown in Figure 4.12b.

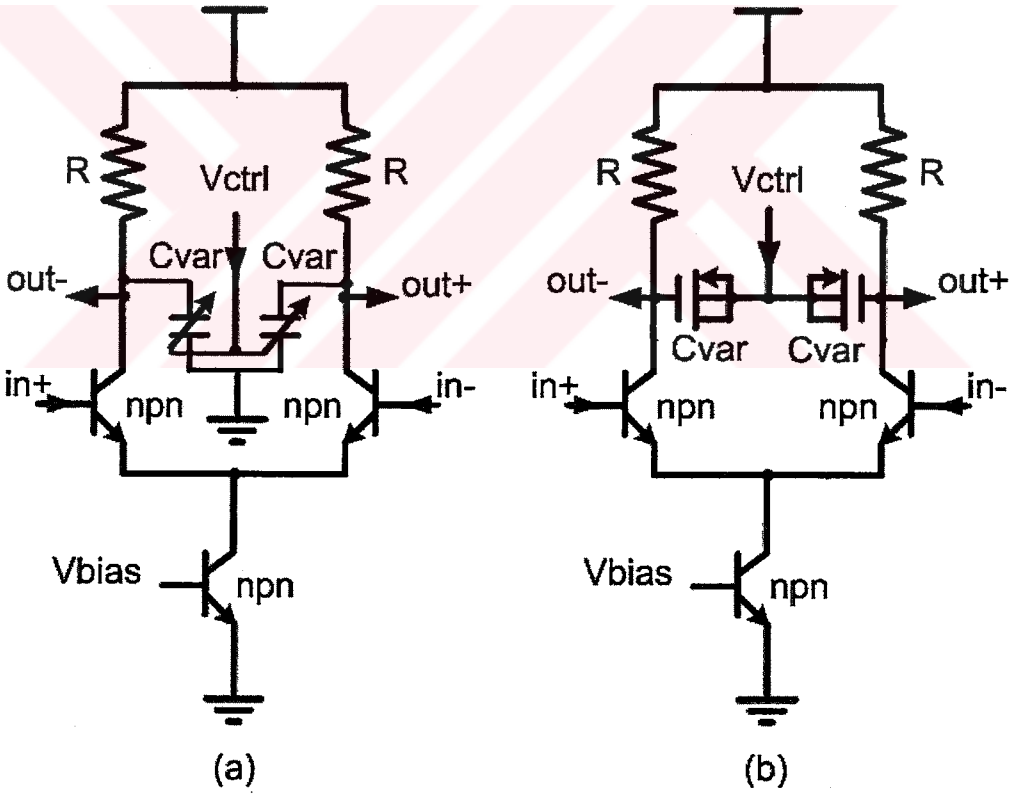


Figure 4.12 Delay stage schematic

Basic HBT current steering stage, called gate delay, experiences a minimum delay of below 20ps for fully switching differential input. This value can be lowered further by reducing the load resistor values and increasing the tail current. Minimum delay value for an NMOS stage is about 80ps, which is five times of the HBT stages. Keeping in mind that for 4GHz clock

signal, reference signal period is only 250ps, such a stage experiencing comparable amount of delay is not appropriate as a delay stage.

Consider a delay stage having a minimum (constant) delay of 80ps and a variable portion of 25ps. According to chapter 2.4, in order to achieve enough capture range for the DLL, minimum 10 delay stages has to be used. Thus total VCDL delay can be calculated with equation (2.15), which is repeated here for clarity and if each stage is identical;

$$T_d = \left[\sum_{i=1}^{n} T_{dps,i}\right] = \sum_{i=1}^{n} \tau_{dps,i} + \sum_{i=1}^{n} \Delta\tau_{dps,i} = (\tau_{dps} \times n) + (\Delta\tau_{dps} \times n) \tag{4.15}$$

where τ_{dps} is the constant delay and $\Delta\tau_{dps}$ is the variable portion of the delay stage and n is the number of identical delay stages. If we put the values of above example, total delay of voltage controlled delay line becomes;

$$T_d = \left[\sum_{i=1}^{10} T_{dps,i}\right] = \sum_{i=1}^{10} \tau_{dps,i} + \sum_{i=1}^{10} \Delta\tau_{dps,i} = (80ps \times 10) + \Delta(25ps \times 10) = 800ps + \Delta 250ps \tag{4.16}$$

this result mandates that, DLL can only be locked to the fourth cycle edge of the reference signal, that is why the VCDL cannot experience a delay lower than minimum delay of 800ps, which can be written as, in the locked condition;

$$T_d = 4 \times 250ps = 800ps + \Delta 200ps \tag{4.17}$$

thus this result, m=4, has to be taken into account for calculating the loop dynamics and stability constant explained in chapter 3 (equation 3.15). Thus stability of the loop can considerably be affected by the higher values of minimum delay of one delay stage.

Above example shows that, lower minimum delay values especially lower than reference period ($T_{ref}=1/f_{CLK}$) may allow the DLL to lock lower number of cycles of the reference signal, desirably equal to one.

It should be noted that, if the variable portion of the stage delay is reduced, number of delay stages should be increased, which has to be taken into account while calculating the number of cycles to be locked and the stability of loop. Also, increased number of delay stages results more timing jitter at the output of the VCDL according to [Weigandt, C. and Kim, B. and Gray, P. 1994] and explained in noise properties of DLL section;

$$\sigma^2_{VCDL} = N.\sigma^2_{jps} \tag{4.18}$$

where σ^2_{VCDL} is the variance of the VCDL output timing jitter, σ^2_{jps} is the variance of the delay stage output timing jitter ($=\Delta\tau^2_{jps}$) and N is the number of delay stages. Subscript "jps" refers to "jitter per stage" and should not be confused with the "variable delay portion of delay stage" ($\Delta\tau_{dps}$).

Thus it is important to have small minimum delay and large variable delay at the delay stages, in order to have naturally stable and excellent noise behavior of DLLs. Delay stage design procedure rely on above problems and trade-offs so varactor design that determine the variable portion of the delay stages becomes more important, in order to get desired performance from the DLL.

4.3.2 Varactor Design

Varactors can be implemented as diode-varactor or NMOS varactor or PMOS varactor. MOS capacitors are widely used in modern silicon technologies. Varactor implementations rely on MOS capacitors with connecting the bulk, drain and source terminals together and controlling the biasing conditions (V_{BG}) and so their working regimes resulting different amount of capacitance. Used technology in this design does not have twin or triple well which prevents the implementation of NMOS varactors. Diode varactors are not chosen because of their lower tuning range and poor phase noise performances [Andreani, P. and Matisson, S., 2000]. Thus PMOS varactors are interested ones.

In PMOS capacitors, an inversion channel with mobile holes builds up for $V_{BG}>|V_T|$, where $|V_T|$ is the threshold voltage of the transistor. The condition $V_{BG}>>|V_T|$ guarantees that the MOS capacitor works in the strong inversion region, the region where the MOS device shows a transistor behavior. On the other hand, for some voltage $V_G>V_B$, the PMOS transistor enters the accumulation region, where the voltage at the interface between gate oxide and semiconductor substrate is positive and high enough to allow electrons to move freely. Thus, in both strong inversion and accumulation region the value of the PMOS capacitance C_{mos} is equal to oxide capacitance, $C_{ox}=\varepsilon_{ox}.S/t_{ox}$, where ε_{ox} is the dielectric constant of the oxide, S is the channel area of transistor and t_{ox} is the oxide thickness.

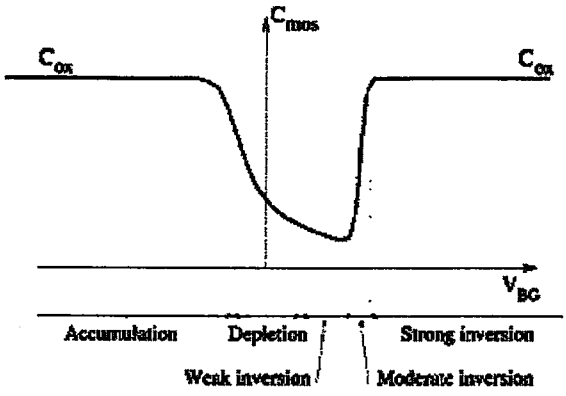


Figure 4.13 Tuning characteristics for the PMOS capacitor with bulk, drain and source terminals shorted (B≡D≡S).

Three more regions can be distinguished for intermediate values of V_{BG}, which are moderate inversion, weak inversion and depletion regions (Figure 4.13). In these regions there are few or very few mobile charge carriers at the gate oxide interface, which causes a decrease of the capacitance C_{mos} of the PMOS transistor. Thus, C_{mos} can be separated to three different capacitors; C_{ox} is in series with the parallel of modulation of the depletion region below the oxide and variation of the number of holes at the gate oxide interface. If the depletion region capacitance dominates the gate oxide interface hole capacitance, PMOS transistor is working in the depletion region, if neither capacitance dominates device works on weak inversion region.

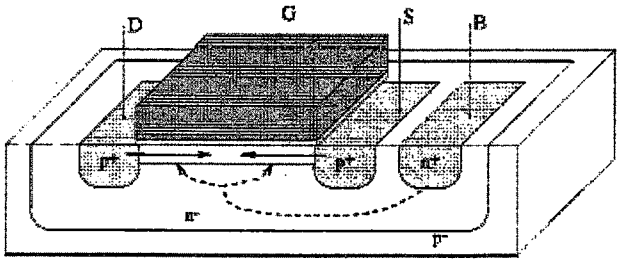


Figure 4.14 Charge carrier path for PMOS capacitor working in the strong and moderate inversion regions (solid lines) and in the depletion and accumulation regions (dashed lines).

These regions results different parasitic resistances that affects the quality factor of the capacitor. Figure 4.14 shows charge carrier path for different regions of the PMOS transistor shown in Figure 4.13. Considering strong and moderate inversion regimes, majority charge carrier flow through drain and source terminals. If bulk terminal is connected to highest dc-voltage V_{DD}, than accumulation region is restricted and varactor can be tuned between depletion and strong inversion regimes, which is called inversion mode PMOS varactor.

In depletion region, parasitic resistance is associated with the resistive losses of electrons moving from bulk contact to the interface between bulk and physical depletion layer (dashed lines in Figure 4.14) which result lower parasitic resistance than the strong inversion regime. If bulk, drain and source terminals connected together, all inversion regions are restricted, meaning that suppression of any injection of holes to the MOS channel. This results a variable capacitor working in the accumulation and depletion regions depending on the V_{BG} voltage.

Lower parasitic resistances (R_p) of accumulation mode PMOS varactors experience better quality factor (Q). That is;

$$Q = \frac{1}{2\pi f C_{mos} R_p} \tag{4.19}$$

Tuning range of varactors is defined as;

$$\gamma = \frac{C_{max} - C_{min}}{C_{max} + C_{min}} = \frac{\Delta C_{tune}}{C_{max} + C_{min}} \tag{4.20}$$

Looking into Figure 4.13 more closely, inversion mode varactors give more linear tuning range but in very short range. This can cause problems for delay stages and the DLL because possible disturbances and noises on the control voltage or VCDL can prevent the loop to be locked. Wider loop bandwidths are avoidable in that case that cause poor noise performance as explained in chapter 2. Accumulation mode varactors draws lower current and offer more tuning range thus, a linear portion can be chosen, which result better delay stage and loop performance besides its higher Q values than the inversion modes.

In order to have higher tuning range or C_{max}/C_{min} channel length, L, of the PMOS transistor can be increased but this gives an increase to the parasitic resistance that lowers the Q. Thus tuning range and Q are inversely proportional. Also phase noise is proportional to Q [Andreani, P. and Matisson, S., 2000]. Besides increasing channel width, W, parallels more varactors but C_{max}/C_{min} ratio remains unchanged. The trade-off here is whether choosing wider tuning range resulting more variable delay portion for the delay stages or good noise performance.

Varactor capacitance values are directly dependent on operating frequency. The AC capacitance seen from the gate and the parasitic resistance of the varactor has to be calculated carefully. Parasitic resistance of accumulation mode varactors grows linearly with the increasing frequency thus Q depends on not only tuning range but the operating frequency.

The selection here is made upon the choice of C_{max}/C_{min} ratio that gives more variable delay portion for a delay stage but minimum delay has tried to be kept in a range that is lower than a couple of number of reference cycles for the VCDL. Gate voltage is an important factor determining the varactor characteristics such as control voltage range changes for different gate biasing conditions. Also large signal swings at the gate of the varactor, can change the capacitance value according to gate voltage swing, which result an unwanted delay variation in the delay stage [Hegazi, E. and Abidi, A., 2003]. The unwanted delay variations caused by the larger voltage swing at the gate of the PMOS varactor, shows up as jitter at the VCDL output. Keeping in mind that, larger voltage swings results lower jitter, this trade-off has to be managed carefully.

Designed accumulation mode PMOS varactor has C_{max}/C_{min}=815fF/274fF≈2.97 ratio and tuning range γ=0.497 at 4GHz operating frequency which is built up with channel length, L=1.5μm and channel width, W=120u. Wide accumulation mode PMOS varactor is separated into pieces those implemented in same n-well connected parallel. Simulated figures below show trade-offs between biasing conditions, channel lengths and tuning ranges for designed accumulation mode varactors.

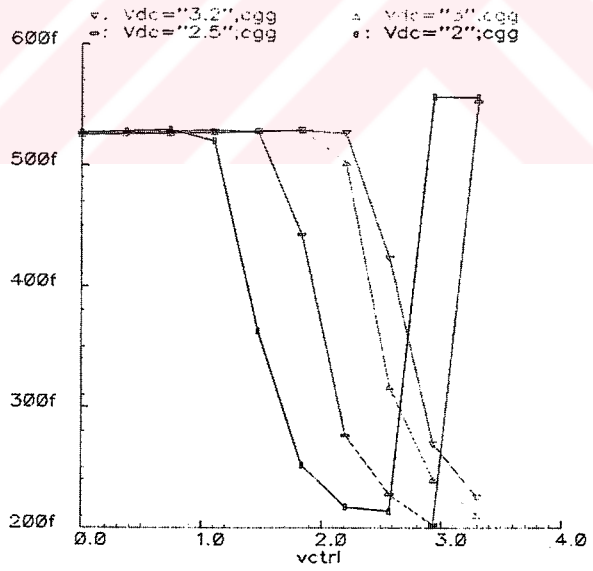
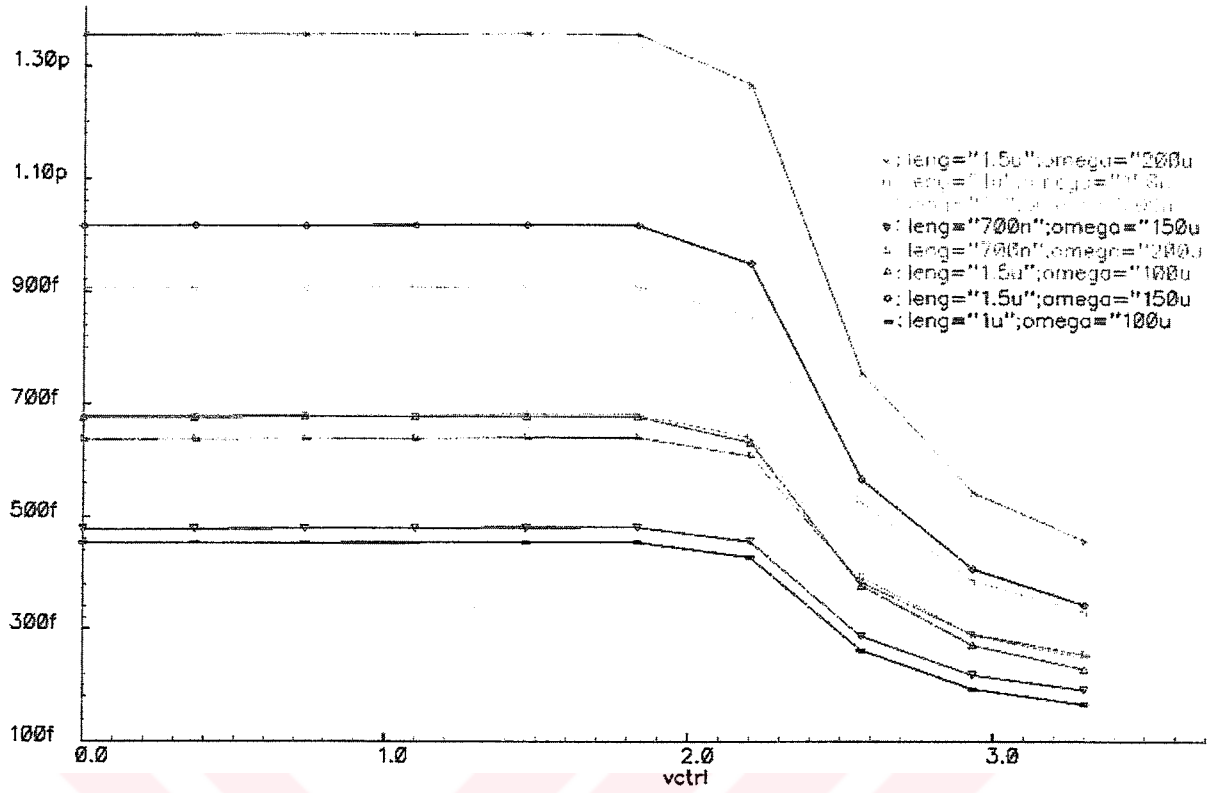
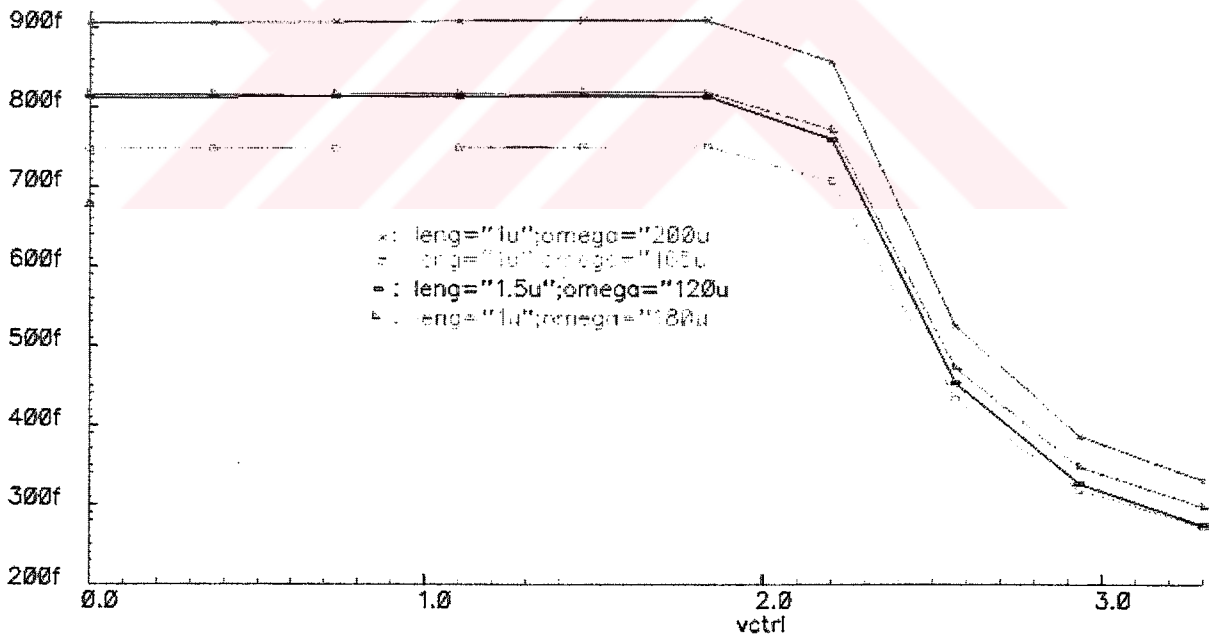


Figure 4.15 capacitance vs control voltage for different gate voltage biasings



(a)



(b)

Figure 4.16 Capacitance vs control voltage with different channel lengths

4.3.3 VCDL Design

Basic delay stage constructed with accumulation mode PMOS varactors those have tuning range γ=0.497 or the ratio C_{max}/C_{min}=815fF/274fF≈2.97, is shown in Figure 4.17. When minimum of three cascaded delay stages combined together in order to provide proper loading conditions for preceding and following stages, a delay stage experiences a minimum delay of about 36ps for C_{min} and a maximum delay of about 55ps resulting a variable delay below 20ps when the stage is biased at typical DC condition which is 2mA tail current and 100Ω load resistors, thus 200mV_{pp} voltage swing and DC gate biasing of the varactor becomes 3.2V. Although, having C_{max}/C_{min} ratio greater than one at the operating frequency and linear relationship between stage delay and load capacitances which is derived in equations 4.11 and 4.14, simulated gate delay ratio $T_{dps,max}/T_{dps,min}$=55ps/36ps is lower than 2. This is why, load capacitances are not formed only from varactors, but following stage input capacitance also has to be taken into account when relating the $T_{dps,max}/T_{dps,min}$ ratio and C_{max}/C_{min}. Thus,

$$\frac{T_{dps,max}}{T_{dps,min}} = \frac{C_{max} + C_{in}}{C_{min} + C_{in}} \tag{4.21}$$

where C_{in} denotes for the following stage parasitic input capacitance. According to above result and putting the varactor capacitance and delay values, a back annotated calculation can be done in order to predict the parasitic input capacitance of the following stage, which brings the parasitic capacitance at the output node about C_{in}≈745fF. This value is higher than the actual physical parasitic capacitances of the input node of the following stage, but if take miller capacitance of the following stage into account, which is determined by the voltage gain, a_v, times the base-collector parasitic capacitance, C_{bc}, above result is equal to input node parasitic capacitances of the following stage. These calculations are verified with the simulations.

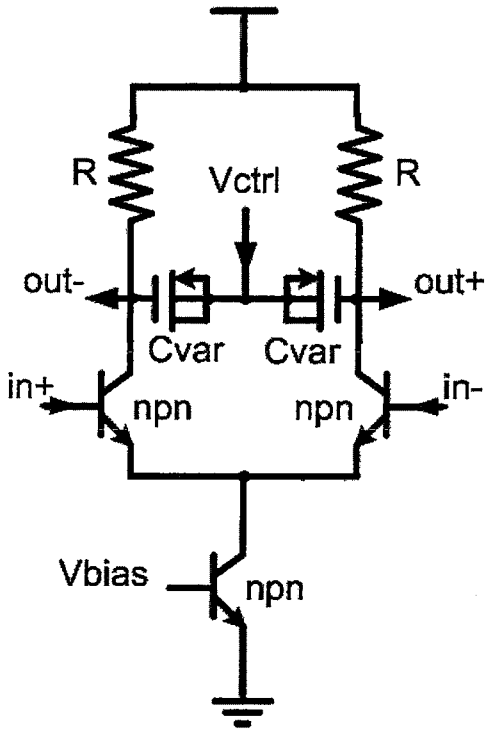


Figure 4.17 Basic delay stage

Decreasing stage small-signal gain, a_v, can reduce miller capacitance and thus loading of the preceding stage, but lowering a_v below unity has to be avoided for the sake of signal maintenance throughout the delay chain. Upper limit for the a_v is determined by the parasitic miller capacitance but more importantly increased jitter contribution. It is well known that, a noise voltage at the input of a stage is amplified to the output with the small-signal gain, a_v. This yields higher output jitter for the VCDL than expected in the equation (4.18). Thus, small-signal gain of the delay stage has to be chosen a few above the unity for all PVT conditions. In fully-switching stages this result is invalid because small-signal gain definition becomes irrelevant while the stage is fully switched.

Basic delay stage implementation has another drawback when the varactor capacitance value rises to its top value. Besides, high equivalent parasitic input capacitance of the following stage gives more raise to the total capacitance at the output node of the delay stage which is almost equal to 1.5pF. Tail current becomes insufficient while discharging the high value capacitor, thus voltage swing decreases with the increasing varactor capacitance, which can prevent fully switching of the following stages, if cascaded numbers of delay stages in a chain is concern, which is the case for a VCDL. In order to maintain constant signal levels, more tail current has to be supplied. Keeping load resistors constant in this case, highly increased tail current give rise to small-signal gain at the same order of magnitude whose unwanted

consequences are explained before. But implementation hardness of such a feedback system replica feedback bias and effective load resistance adjusting for variable delay at operating frequency of 4GHz, give only the chance of tuning tail current. Thus this mechanism has to be handled carefully by keeping in mind the consequences of this solution.

Some modifications have to be made on basic delay stage in order to maintain signal integrity and have more adjustable delay per delay stage. As first sight, to prevent effects of higher input parasitic capacitance value of the following stages emitter followers (EFs) come as solution (Figure 4.18). If the BV_{CEO} condition is avoided, EFs can isolate two cascaded stages and significantly reduce the parasitic capacitance resulting lower minimum delay and higher delay ratio despite introduce more delay to the ongoing signal. Simulation results show that delay values and $T_{dps,max}/T_{dps,min}$ delay ratio remains almost the same with the previous delay stage, which means that income from increased C_{max}/C_{min} ratio and reduced parasitic capacitance of the next stage (C_{in}), is paid to the EF delay. But the benefit comes from the voltage swing considerations. This time, voltage swing is a little reduced with respect to the basic delay stage because of the reduction of total maximum capacitance at the output node ($C_{max}+C_{in}\approx 810fF+200fF$), that is almost reduced to 1pF (which was 1,5pF for basic delay stage). Thus this feature, which comes up with EFs, allows the use of lower additional tail current levels to recover the voltage swing with the increasing varactor capacitance ($2mA+I_{tune}$). Thus lower amount of increase in small-signal gain caused from the lower additional tail current is preferable rather than previous delay stage case.

It should also be noted that calculations of capacitances for output nodes captures the parasitic element models that are caused by the layout. Model values are extracted from the typical interconnect layouts for the stages.

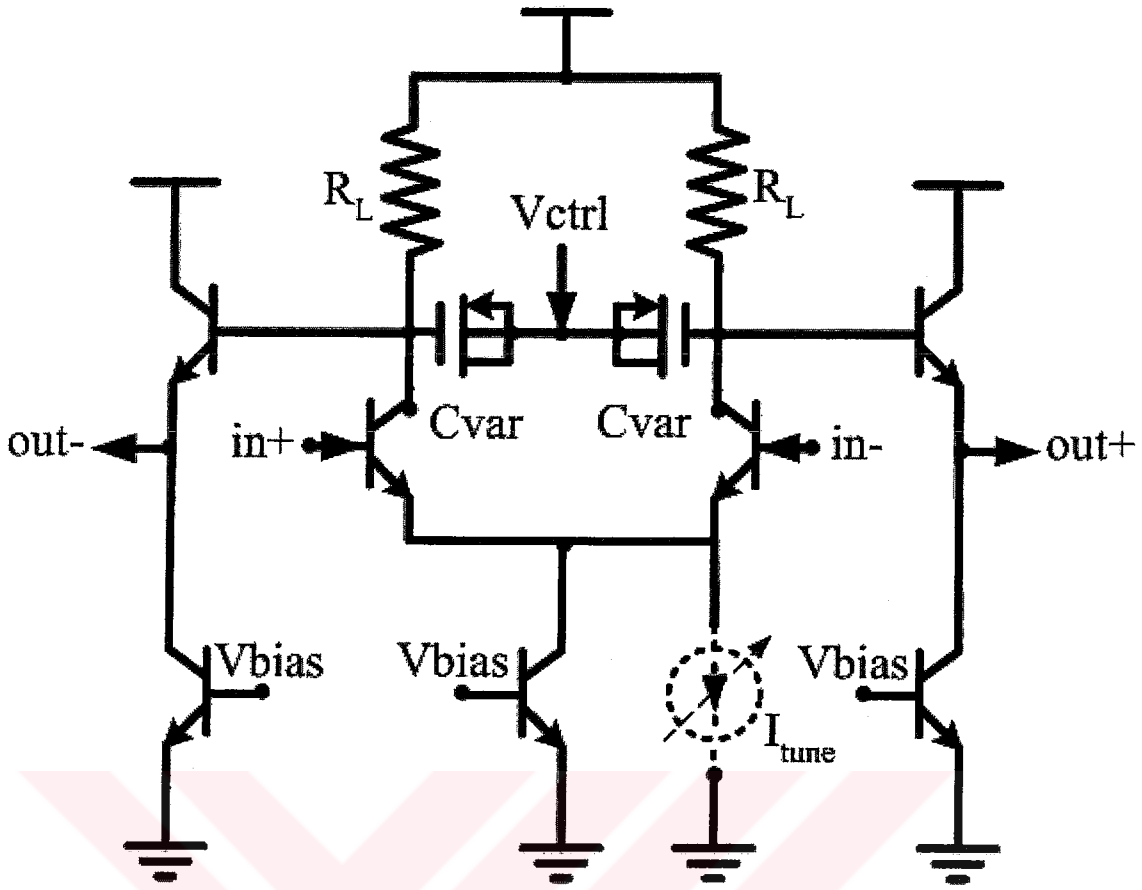


Figure 4.18 Modified delay stage.

EFs suffer from ringing phenomenon, which can be called as inductive behavior with the increasing frequency caused by the high input resistance values seen at the output at high frequencies which is shorted to output with C_{be} capacitance and lower resistance values seen at the output of r_e=1/gm at lower frequencies where C_{be} is open circuit. This situation is visualized in Figure 4.19. the output impedance of the stage can be written as;

$$Z_{out} = \frac{1 + s.R_s.C_{be}}{gm + s.C_{be}} \tag{4.22}$$

According to above output impedance equation, in case of using lower input resistance values even at high frequencies, ringing can be minimized (Figure 4.19c). In this design, EFs do not experience considerable ringing. It should also be noted that, AC base currents of EF loads, could steal EF tail current, which might result improper operation for the stage thus should be carefully avoided.

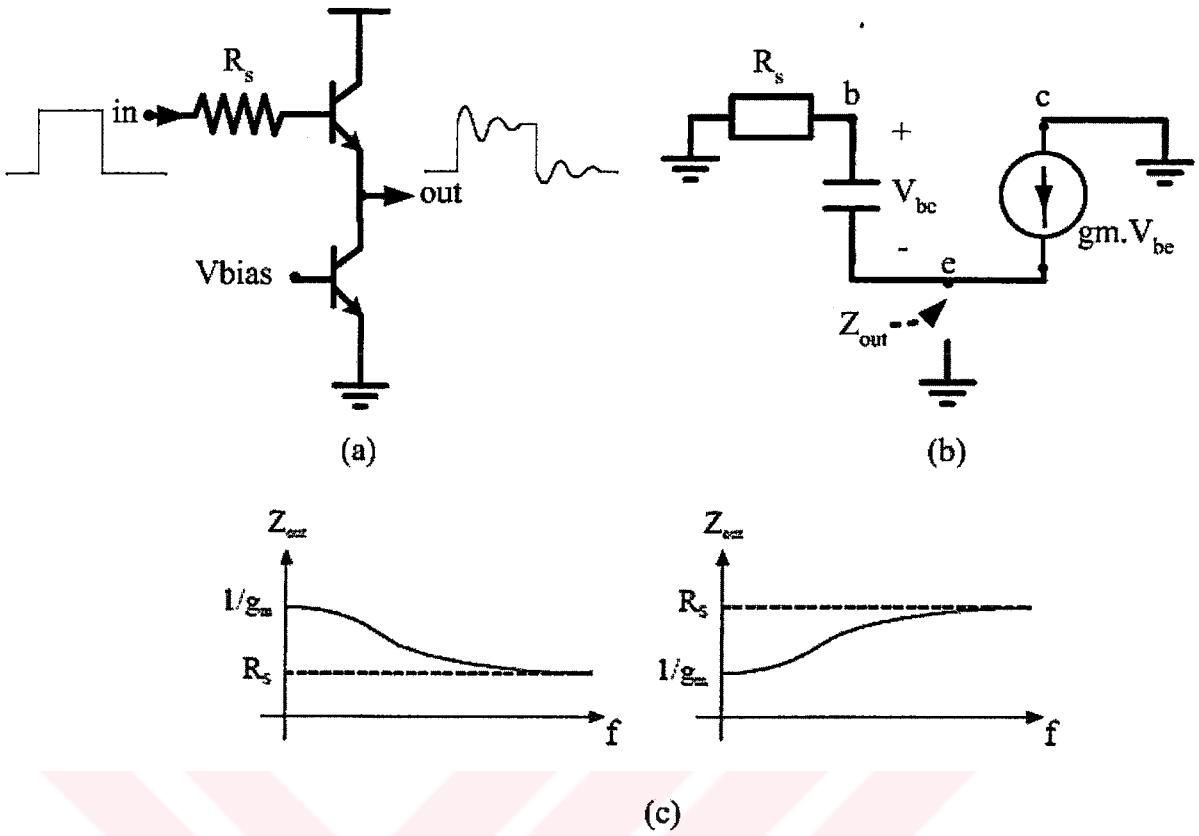


Figure 4.19 Ringing phenomenon (a) an emitter follower experiencing ringing on the output signal (b) small-signal equivalent of emitter follower (c) output impedence vs frequency for $R_s<r_e$ and $R_s>r_e$ respectively

Emitter follower delay is also adjustable by controlling the tail current. EFs can have up to 7-8ps additional variable delay without sacrificing the signal condition. Thus allows use of less number of delay stages in the VCDL. But this feature is not used in implementation of the delay stage, because of the testing purposes that will be explained later which are briefly, occupied edge combiner circuits and possible usage of the DLL as multiphase clock source that loads the delay stage outputs and reducing EF tail currents introduces some problems while driving such loads.

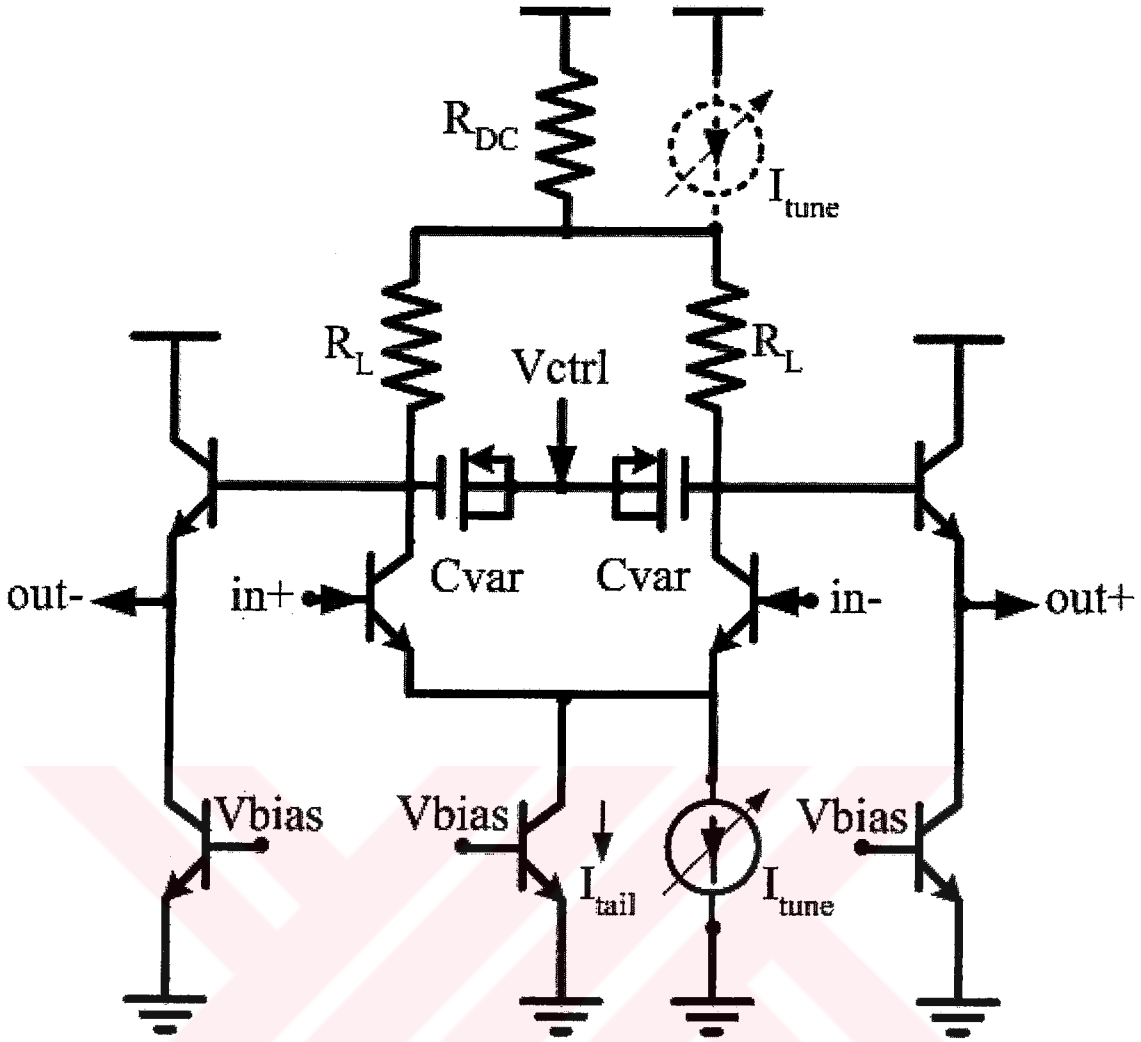


Figure 4.20 Delay stage implementation.

In order to reduce minimum delay of the stage shown in Figure 4.18, a speed-up resistor, R_{DC} is added to the delay stage as shown in the Figure 4.20, which also reduces the common mode voltage level of the output signal and can be used to manipulate DC biasing condition of the stage in order to prevent any breakdown of the high speed HBT modules. Stage also incorporates additional tail current source, which supplies an amount of current depending on the varactor capacitance in order to keep output voltage swing constant. But this additional tuning current cause a control signal dependent common mode voltage variation at the output of the delay stage, whose consequences has to be examined.

Finalized delay stage, shown in the Figure 4.20, biasing condition as follows; I_{tail}=2mA, variable tuning current I_{tune} is between 0-1.5mA, R_L=110Ω and R_{DC}=200Ω and also HBT devices in active region experiences base-emitter voltage, V_{be}, a little above 800mV under typical biasing conditions.

Common mode voltage level of the output signal can be written as;

$$V_{cm,out} = V_{DD} - \left[\left(R_{DC} + \frac{R_L}{2}\right).(I_{tail} + I_{tune}) + V_{be,EF}\right] \quad (4.23)$$

according to above biasing conditions and equation (4.23) and for the two extreme cases for tuning current, common mode voltage variation of the delay stage is approximately 350mV. This value does not cause problems, while driving the cascaded stage and any breakdowns. Changing common mode output level of the cascaded delay stages and so as the VCDL, is not troublesome for the phase/frequency detector because of the incorporated buffer stages that arranges proper common mode and voltage swing of the signal for PFD. But this dependency changes the varactor gate DC biasing condition thus tuning range of the varactor, which can be eliminated by placing a current source in parallel with the R_{DC} with the same additional amount with I_{tune} (dashed current source in Figure 20). Thus additional current cannot flow through R_{DC} and cause common mode voltage level change. It is possible to modify the charge pump output buffer in order to arrange the differential control voltage common mode level with the same amount, but this can cause stability problems for the loop and thus is not examined further.

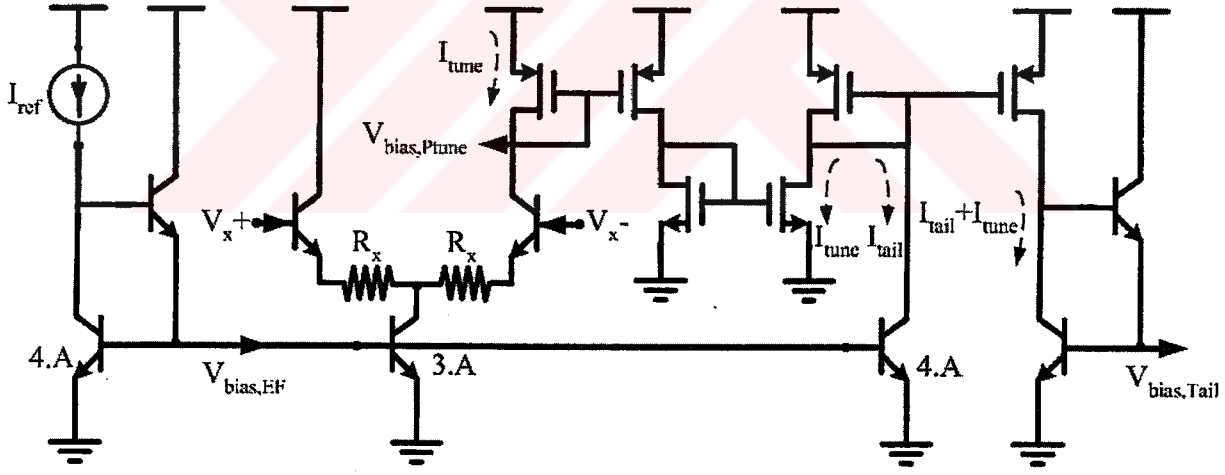


Figure 4.21 Voltage controlled delay line biasing scheme.

Current sources are implemented with high voltage HBT modules as mentioned before. Degeneration resistors that improve current matching are not used in the current mirrors because of their additional thermal noise contribution and voltage headroom problems result from high current levels. Biasing scheme of the VCDL is shown in Figure 4.20. Reference current is supplied from master bias circuit (2mA), constant emitter follower currents are copied from $V_{bias,EF}$ (1mA), constant portion of tail currents (2mA) of the delay stages is

summed with variable portion (0-1.5mA) and copied as $V_{bias,tail}$ and variable portion is also copied as $V_{bias,Ptune}$ in order to implement dashed I_{tune} in Figure 4.20.

I_{tune} has to be supplied to the delay stage according to control voltage, V_{ctrl}, produced from the charge pump and the loop filter that adjusts varactor capacitance and thus VCDL delay. As the varactor capacitance increases with the control voltage, tuning current has to increase in the same direction with an amount that keeps the voltage swing constant. This tuning current has to have linear control range, as same as the linear control range of the varactors. A degenerated common emitter stage is used for this purpose as shown in Figure 4.21. Level shifted version of the control voltage from the charge pump, V_x+ and V_x-, directs the tail current (1.5mA) either to a PMOS current mirror or V_{DD}, linearly. Then this additional current is copied to delay stage in order to keep voltage swing constant. This feed-forward approach cannot compensate supply noise effects on the voltage swing but capacitive loading effects. Same amount of linearity cannot be achieved with a first order approach for the tuning current and varactor capacitance but achieved results make us satisfied for the sake of signal maintenance throughout the VCDL (Figure 4.22). Resulting voltage swing variations depending on the control voltage level for VCDL is $20mV_{pp}$.

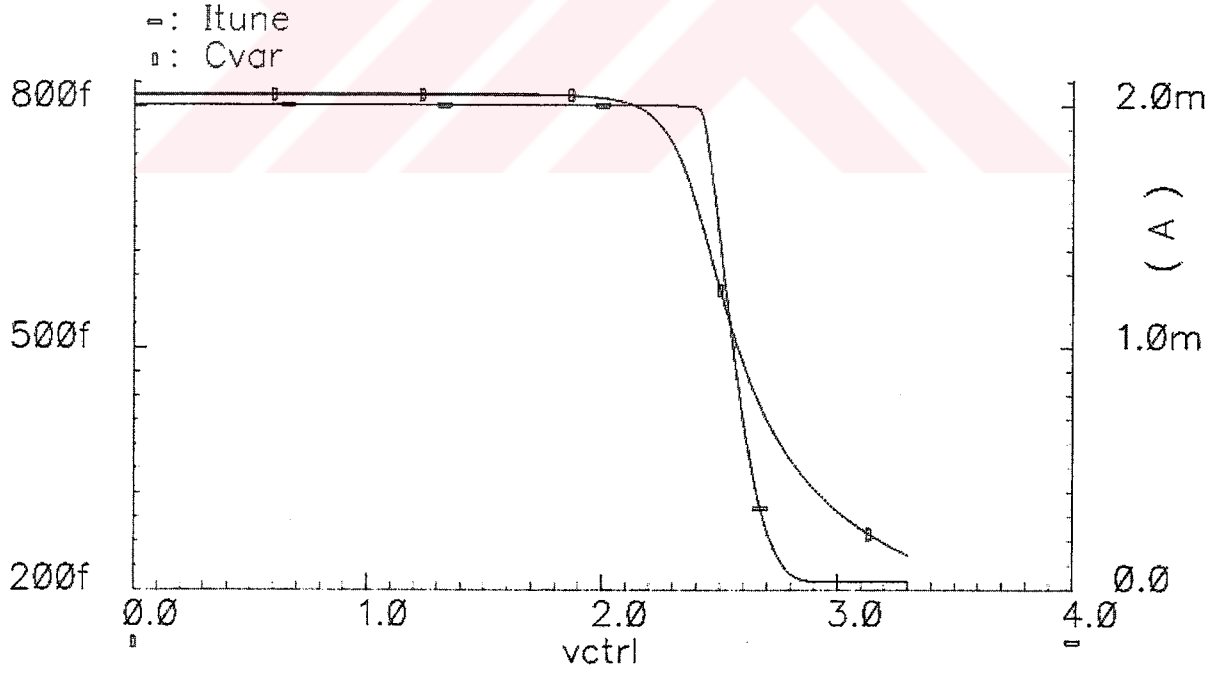


Figure 4.22 Tuning current and varactor capacitance versus control voltage

Finalized delay stage experiences a delay between 33ps (τ_{dps}) and 56ps. Variable delay portion of a delay stage becomes $\Delta\tau_{dps}$=56ps-33ps=23ps. The minimum required number of delay stages has to be used in the VCDL can be found by T_{ref}/23ps=250ps/23ps=10.85

resulting n=11. Number of delay stages is chosen to be n=12 for multiphase clocking and frequency multiplication purposes for a test chip. Thus total VCDL delay can be written as;

$$T_d = \left[\sum_{i=1}^{n} T_{dps,i}\right] = \sum_{i=1}^{n} \tau_{dps,i} + \sum_{i=1}^{n} \Delta\tau_{dps,i} = (\tau_{dps} \times n) + (\Delta\tau_{dps} \times n)$$

$$T_d = (33ps \times 12) + (23ps \times 12) = 396ps + \Delta 276ps \quad (4.24)$$

The achieved result suggests that DLL cannot lock the first cycle of the reference period but minimum of second, m=2. The total variable delay of the VCDL, Δ276ps is higher enough in order to achieve proper lock range for the DLL at 4GHz reference frequency. Thus VCDL gain can be calculated now,

K_{VCDL}=2.208.π rads/sec=6.936 rads/sec (4.25)

Variable delay amount has to be kept higher than the reference period under all PVT conditions, which have accomplished because of the nature of the designed varactors because varactors tuning range is constant for PVT variations although minimum and maximum capacitance values have changed. More important point here is the minimum delay variations under extreme PVT conditions, which is always between the 250ps and 500ps thus value "m" remains unchanged.

In locked condition, total VCDL delay will be equal to T_d=500ps. VCDL accommodates a second zero phase shifted node besides its output with respect to reference, that is the midpoint of the VCDL, sixth delay stage output. With the aid of this feature DLL can synchronize 3 different systems by itself in skew cancellation application, one clock source is the input node of the VCDL, one is the sixth stage output and the other is VCDL output (twelfth stage output).

Occupied twelve delay stages divide total VCDL delay equally resulting 500ps/12=41.66ps (0.33π rads) phase shift at cascading delay stage output. This option of the DLL can be used in 6-way multiphase clocking applications. Considering a 6-way time-interleaved ADC, each ADC working on 4Gsps, resulting configuration is at the sample rate of 6×4Gsps=24Gsps. These sample rates are not available for commercial process technologies but can only be achievable for high technology laser or mechanical implementations.

Achieved six equally phase shifted versions of reference clock signal, allow frequency multiplication factor of F=6, which results 6×4GHz=24GHz output clock frequency.

Considering each building block of the DLL can work up to 6GHz reference signal frequency, theoretically 36GHz output clock frequency is achievable (But this frequency is problematic for edge combiner circuit thus 6×5GHz=30GHz case is the concern which will be explained in following sections). In case of using eleven delay stages, according to section 2.5.3 frequency multiplication factor becomes F=n/m=11/2=5.5, thus output clock frequency is equal to 5.5×4GHz=22GHz, if some delay is introduced to system and making m=3, thus F=3.66 resulting 14.66GHz. These values can be arranged according to demanded frequency multiplication factor.

4.4 Results

4.4.1 Stability Analysis in s-domain

It is important to examine DLL dynamic behaviors with the procedure given in chapter 3. Combined PFD and charge pump gain filter capacitor value and VCDL gain is (repeated here for convenience);

$$K_{PD\_CP} = \frac{I_{cp}}{2\pi} = \frac{1mA}{2\pi}$$

Cp=275pF

K_{VCDL}=2.208.π rads/sec (4.26)

s-domain open loop gain, G(s), of the DLL becomes;

$$G(s) = \frac{K_{PD\_CP}.K_{VCDL}}{sC_p} = \frac{10^{-3} \times 2.208.\pi}{s.2\pi.275.10^{-12}} = \frac{4.015.10^6}{s} \quad (4.27)$$

Closed loop transfer function of the DLL is;

$$H(s) = \frac{\theta_{out}}{\theta_{in}} = \frac{\omega_n}{s+\omega_n} = \frac{\frac{K_{PD\_CP}.K_{VCDL}}{C_p}}{s+\frac{K_{PD\_CP}.K_{VCDL}}{C_p}} = \frac{4.015.10^6}{s+4.015.10^6} \quad (4.28)$$

Various closed loop dynamic properties of the DLL is shown in Figure 4.23 to 4.25. Step response settling time of the DLL is found to be lower than 1μs. DLL transfer function exhibits a first order system, which is always stable. Zero-pole map of the DLL is shown in

Figure 4.25, showing location of the only one pole of the system. 3-dB cutoff frequency is about 640KHz while charge-pump current is 1mA. As mentioned in charge pump implementation section, tail current source is variable in order to be able to change the loop bandwidth for testing purposes. Bode plots for 1mA and 100μA tail currents have been given in Figure 4.26 for comparison. As expected, reduced charge pump current reduces loop bandwidth about ten times but increases the settling time with the same amount.

In order to be able to test the prototype implementation of the DLL in case of having noisy input signal source, loop bandwidth has to be maximized for the sake of locking. If not DLL could not be able to lock its output to the reference. Noise performance of the DLL will be changed with the changed loop bandwidth.

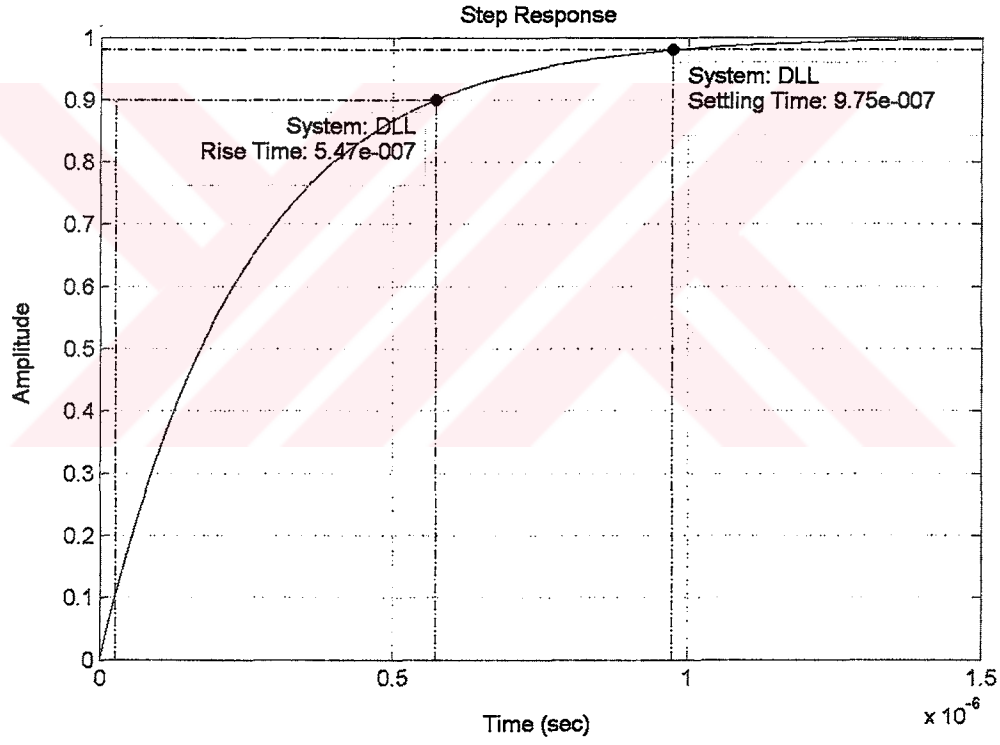


Figure 4.23 Step response of the DLL s-domain model

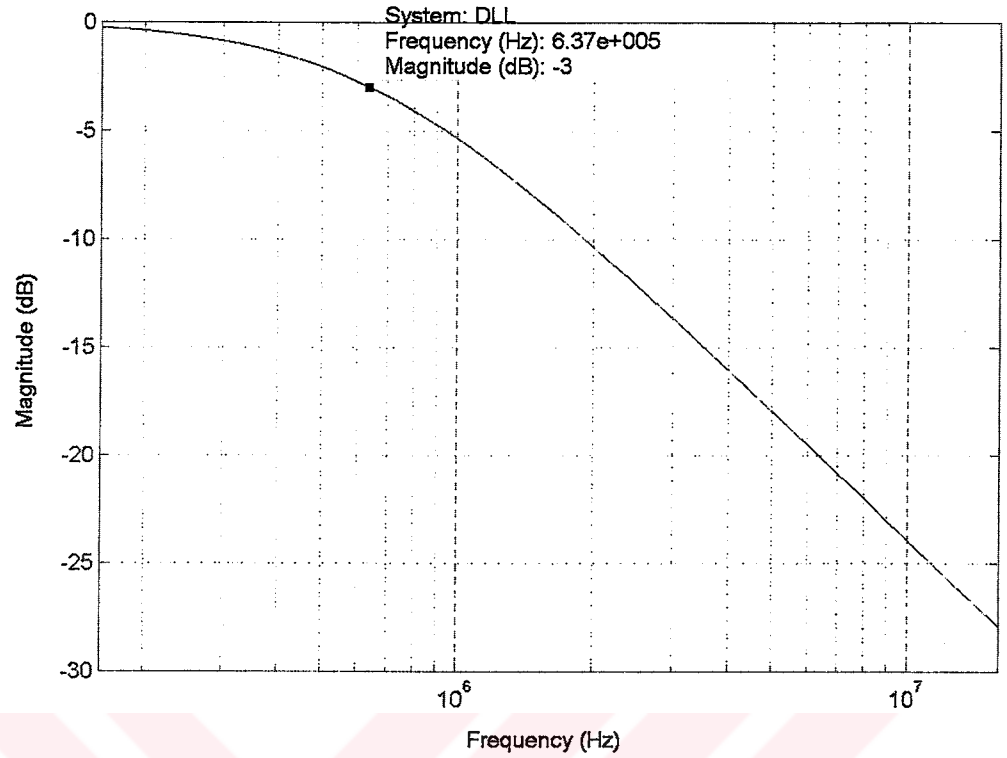


Figure 4.24 Bode plot of the DLL s-domain model

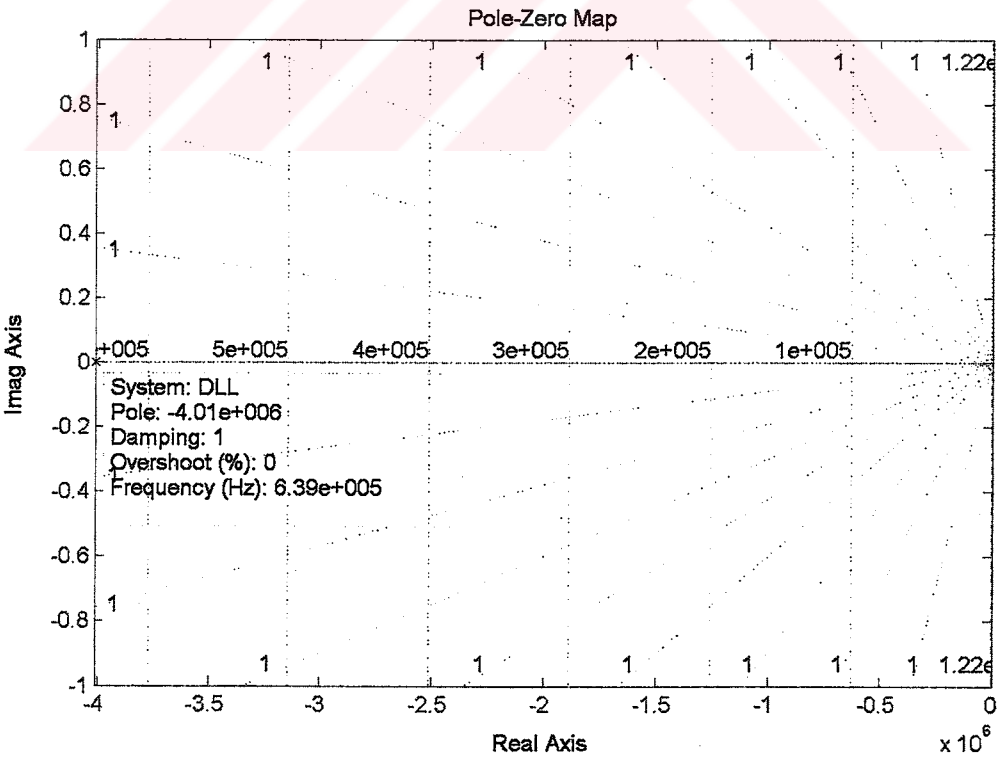


Figure 4.25 Zero-Pole map of the DLL s-domain model

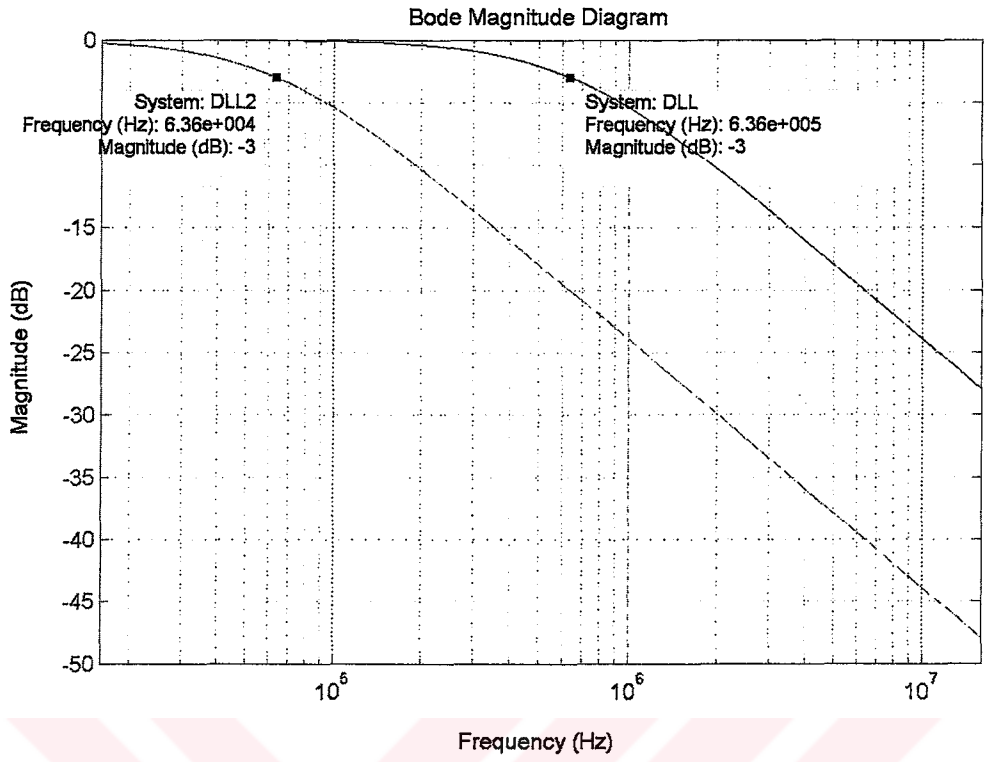


Figure 4.26 Bode plots of DLL s-domain model for I_{cp} 1mA (DLL) and 0.1mA (DLL2)

4.4.2 Jitter Peaking

In order to determine the jitter transfer characteristics of the DLL, discrete-time model is used as explained in chapter 3 (Figure 3.8). Calculated gain values of the loop components have to be arranged for z-domain analyses. Combined phase detector and charge pump gain including loop filter capacitance becomes;

$$K_{PD\_CPz} = \frac{I_{cp}}{\omega_{clk} C_p} = \frac{I_{cp}}{2\pi C_p}.T_{ref} = \frac{1mA}{2\pi 275pF}.250ps = 144.7\times10^{-6} \quad (4.29)$$

also voltage controlled delay line gain is;

$$K_{VCDLz} = K_{VCDL} = 2.208\pi \quad (4.30)$$

Loop gain can be defined as;

$$K = K_{PD\_CPz}.K_{VCDLz} = 1.0036\times10^{-3} \quad (4.31)$$

Thus discrete-time DLL transfer function becomes;

$$H(z)=\frac{\theta_{out}(z)}{\theta_{in}(z)}=\frac{(1+K)z-1}{z-(1-K)}=\frac{1.001z-1}{z-0.999} \tag{4.32}$$

Jitter peaking can be calculated for half of the sampling frequency (refer to chapter 3), which yields;

$$\text{JitterPeaking}=P=\frac{2+K}{2-K}=1.001=8.717\times10^{-3}\,\text{dB} \tag{4.33}$$

which is considerably low as desired. Also it should be noted that lowering charge pump current from 1mA to 100μA would reduce jitter peaking ten times. Figure 4.27 shows jitter transfer curve of the DLL for 1mA charge pump current. Peak value is equal to calculated one in equation (4.34). Peak value of phase shift occurs at loop bandwidth, which is 640KHz.

z-domain transfer function experiences one pole and one zero with the same value, one on the other, thus no stability concerns valid (Figure 4.28).

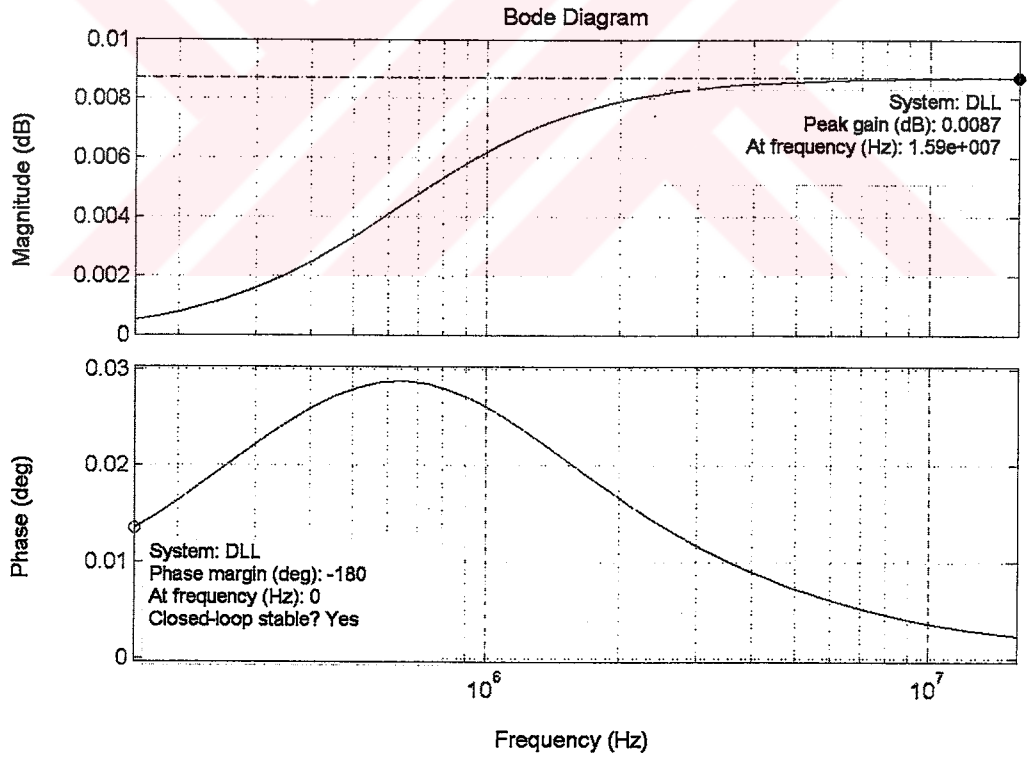


Figure 4.27 Jitter transfer of the DLL

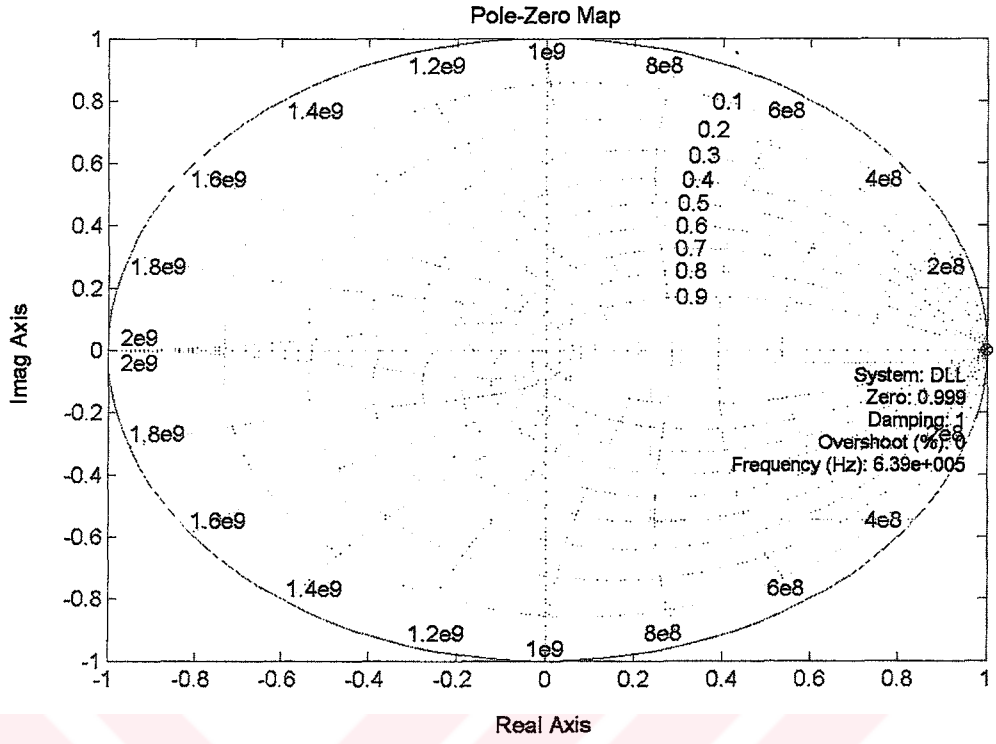


Figure 4.28 Zero-Pole map of the DLL.

4.4.3 Stability Analysis in z-domain

Further stability analysis can be done according to equation (4.34) for m=2 value (chapter 3)

$$H(z) = \frac{\theta_{out}(z)}{\theta_{in}(z)} = \frac{K}{z^m - z^{m-1} + K} = \frac{0.001004}{z^2 - z + 0.001004} \tag{4.34}$$

Discrete-time model represents DLL dynamic behavior more actually. But linearized s-domain model predicts most of the features of the DLL correctly such as loop bandwidth, settling time etc. Figure 4.29, Figure 4.30 and Figure 4.31 derived for z-domain model generally agrees with s-domain calculations given in Figure 4.23, Figure 4.24 and Figure 4.25. One major difference is the second pole introduced to system at 4.4GHz, which can be seen in Figure 4.31. This second pole does not make use to think on any stability precautions.

Two different z-domain models besides the s-domain are used in order to understand the dynamics of the DLL. Each z-domain model represents different behavior one of them is for jitter peaking and the other is loop delay. These two models are combined in order to achieve one model that represents DLL completely but its results are the same with the derived ones here separately. Thus this model is not presented here.

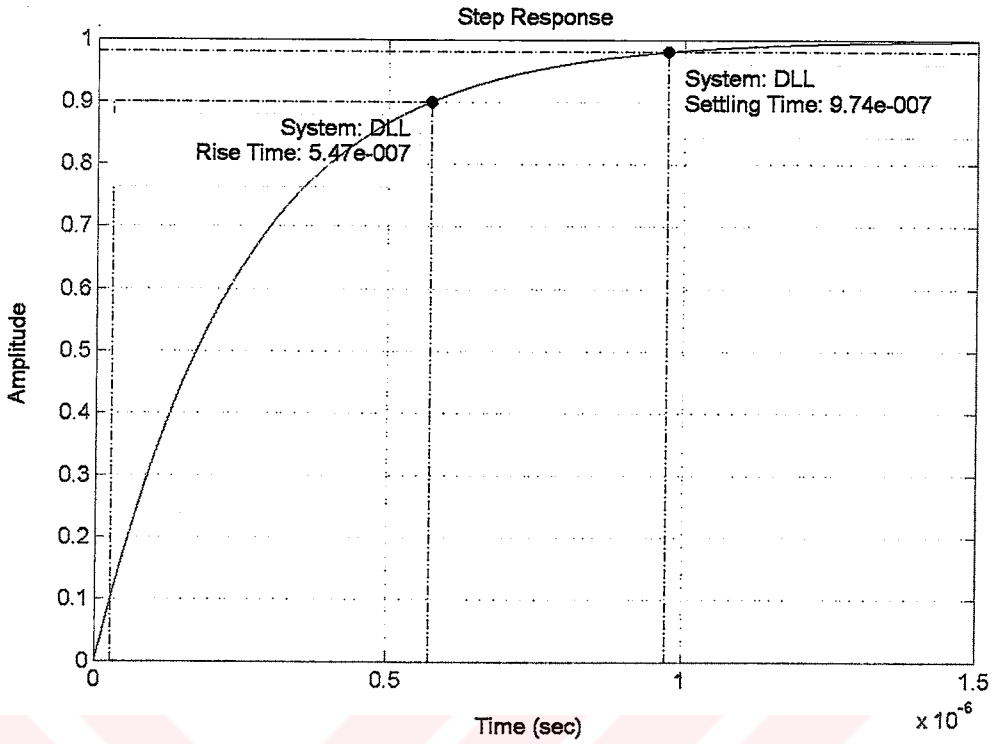


Figure 4.29 Step response of DLL z-domain model

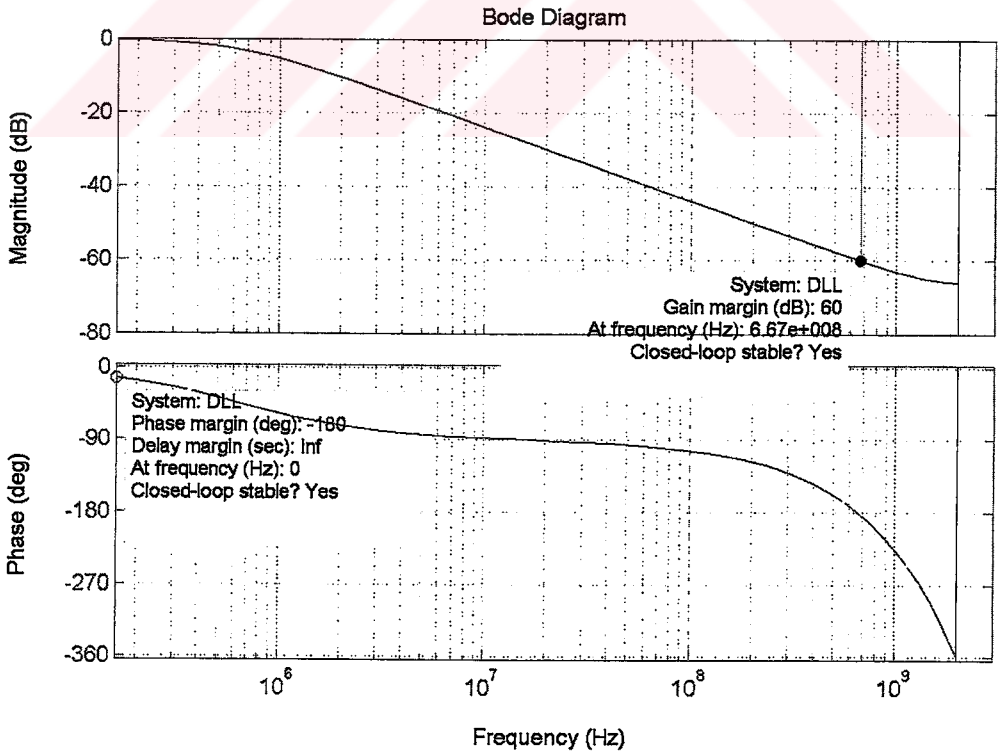


Figure 4.30 Bode plots of DLL z-domain model

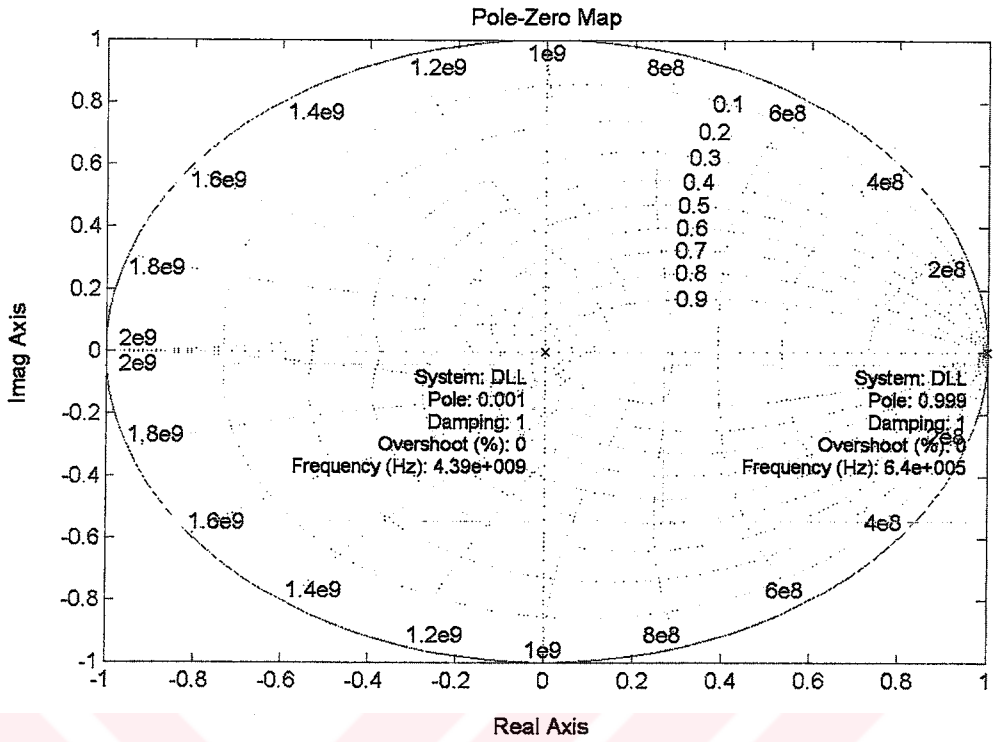


Figure 4.31 Zero-Pole map of DLL z-domain model

4.4.4 VCDL Output Jitter

It is important to calculate the output jitter of the delay stage and thus, total VCDL output jitter. It is important to note that these calculations are made to estimate the performance of the voltage controlled delay line thus some error margin has to be considered.

Using the analytical results in chapter section 3.3.3 with the design parameters given in section 4.3, and constant parameters that are; Boltzmann constant is equal to $k=1.38.10^{-23}$ [Joule/Kelvin], T is the absolute temperature in Kelvin and $q=1.602.10^{-19}$ [Coulomb], each noise contribution of the noise sources in a delay can be found.

Each calculations are made for two extreme cases for varactor capacitances and tail current; at case-1, C_L=300fF and I_{tail}=2mA and at case-2, C_L=820fF and I_{tail}=4mA.

Collector load resistor rms jitter contributions for two extreme cases from (3.27) are,

$$\sigma_{1a} = \sqrt{\frac{2kTC_L}{I_{tail}^2}} = 24.9\text{fs} \qquad (4.35a)$$

$$\sigma_{2a} = \sqrt{\frac{2kTC_L}{I_{tail}^2}} = 20.6fs \tag{4.35b}$$

In tail current calculations, only shot noise is calculated because degeneration resistors are not used. Voltage headroom problems only allow for low value degeneration resistors which increases jitter even above the shot noise contribution. Tail current rms jitter contributions for two cases from (3.36) are,

$$\sigma_{1b} = \sqrt{\frac{q.R_L C_L}{2.I_{tail}}} = 34.6fs \tag{4.36a}$$

$$\sigma_{2b} = \sqrt{\frac{q.R_L C_L}{2.I_{tail}}} = 40.5fs \tag{4.36b}$$

Switching noise is not robust estimation because of the strict assumptions on the equation validity. Also base resistance of the used process is derived under some estimations that is equal to r_{bT}=600Ω for used devices. Thus from (3.45) switching noise for two cases are,

$$\sigma_{1c} = \sqrt{\frac{q.r_{bT}.C_L}{3.I_{tail}}} = 69.3fs \tag{4.37a}$$

$$\sigma_{2c} = \sqrt{\frac{q.r_{bT}.C_L}{3.I_{tail}}} = 81fs \tag{4.37b}$$

The rms fashion jitter values can be summed in order to determine the total output jitter of a single stage for two extreme cases separately. For case-1 and case-2 total output jitter per stage is,

$$\sigma_{ps-1} = \sigma_{1a} + \sigma_{1b} + \sigma_{1c} = 128.8fs \tag{4.38a}$$

$$\sigma_{ps-2} = \sigma_{2a} + \sigma_{2b} + \sigma_{2c} = 142.1fs \tag{4.38a}$$

Total output jitter per stage for two extreme case varies about %0.8. Thus this value is considered to be 130fs for convenience. Total VCDL output jitter can be calculated according to (3.50). For twelve stage VCDL, that is,

$$\sigma_{VCDL} \cong \sqrt{N}.\sigma_{ps} = \sqrt{12}.130fs = 450fs \tag{4.39}$$

In case of occupying ten delay stages, total VCDL output jitter is,

$$\sigma_{VCDL} \cong \sqrt{N}.\sigma_{ps} = \sqrt{10}.130fs = 411fs \quad (4.40)$$

Above results explain the unique noise performance of the DLL. In optimistic point of view, above jitter values that are result of the noise power will be lowered while taking into account that, VCDL output noise power will be filtered by noise transfer function that is given in equation (3.12) while affecting the DLL output. Also these values are derived for uncontrolled VCDL, thus in controlled loop some of the noise power can be reduced. In pessimistic and that is may be more the realistic point of view, the jitter calculation procedure depends on some assumptions which will give rise to these values in reality, and additional elements used in a delay cell are not considered in this calculations. Also these values exclude phase/frequency detector and charge pump jitter contributions, which are assumed to be ignorable.

It is also convenient to know the peak-to-peak jitter value rather than rms jitter. For Gaussian probability distribution function it is well known that, 6σ captures the amount of %99 of the total value, thus for twelve stage VCDL total peak-to-peak jitter is,

$$\sigma_{VCDLpp} \cong 6.\sigma_{VCDLrms} = 2.7ps \quad (4.41)$$

also for ten stage VCDL,

$$\sigma_{VCDLpp} \cong 6.\sigma_{VCDLrms} = 2.46ps \quad (4.41)$$

These calculations have to be cross checked with the simulated noise power values and these calculations has to be improved especially input transistors' base current shot noise and other HBT related noise source contributions. Until the time of the date of today, still noisy model parameters have not been supplied by the factory but only noise parameter documents, which has been guide to the calculations and basic simulations.

The reason for calculating the ten stage VCDL case is for the testing circuit requirements (the edge combiner circuits which are explained in section 5.2) in order to predict the performance of the synthesized output clock for multiplication factor of 5 or 6.

4.4.5 Power Comsumption

It is well known that DLL jitter performance is directly related with power consumption (chapter 3.3), which is kept very high for this application. DLL draws total current of below

100mA capturing extreme case of the VCDL tuning current from supplies excluding DLL input buffer and additional testing circuits (edge combiners, output buffers etc). For typical condition of V_{DD}=3.3V, total power consumption reaches up to 330mW. But it should be noted that, major power hungry block, VCDL (draws the higher than the half of the total current consumption), is designed to have the opportunity of using additional testing circuits. Thus dedicated design for just skew cancellation application, total current consumption of the DLL can be scaled to almost ¾ just with the aid of VCDL by dropping the EFs. Also PFD power consumption can be reduced. In general, for dedicated operation of DLL only at 4GHz, power consumption can further be scaled without sacrificing considerable jitter performance.

4.4.6 Operation

DLL operates properly for 4GHz reference clock frequency. Figure 4.32 shows a transient simulation results with additional control voltage noise source of $20mV_{pp}$ which is added in order to be able to analyze the loop reaction to the noise. In locked condition, differential reference and VCDL output signals experiences zero phase shifts thus up and down signals are equal.

DLL can operate input frequency range of between 3.7GHz and 6GHz properly. For frequencies above 5GHz some control actions have take place, which determines the number of delay stages in the VCDL and also initial conditions for control voltage are determined by the control inputs. These control actions are planned for the testing purposes of the prototype implementation and developments are in progress. Thus in finalized or dedicated implementation for an application a digital control unit can be placed to the IC for digitally controlled autonomous operation or completely removed.

Required simulation times are transient analyses approaches one or two days depending on the desired resolution. Thus complete DLL is simulated for only a few times, but building blocks with properly configured loading situations are characterized distinctively.

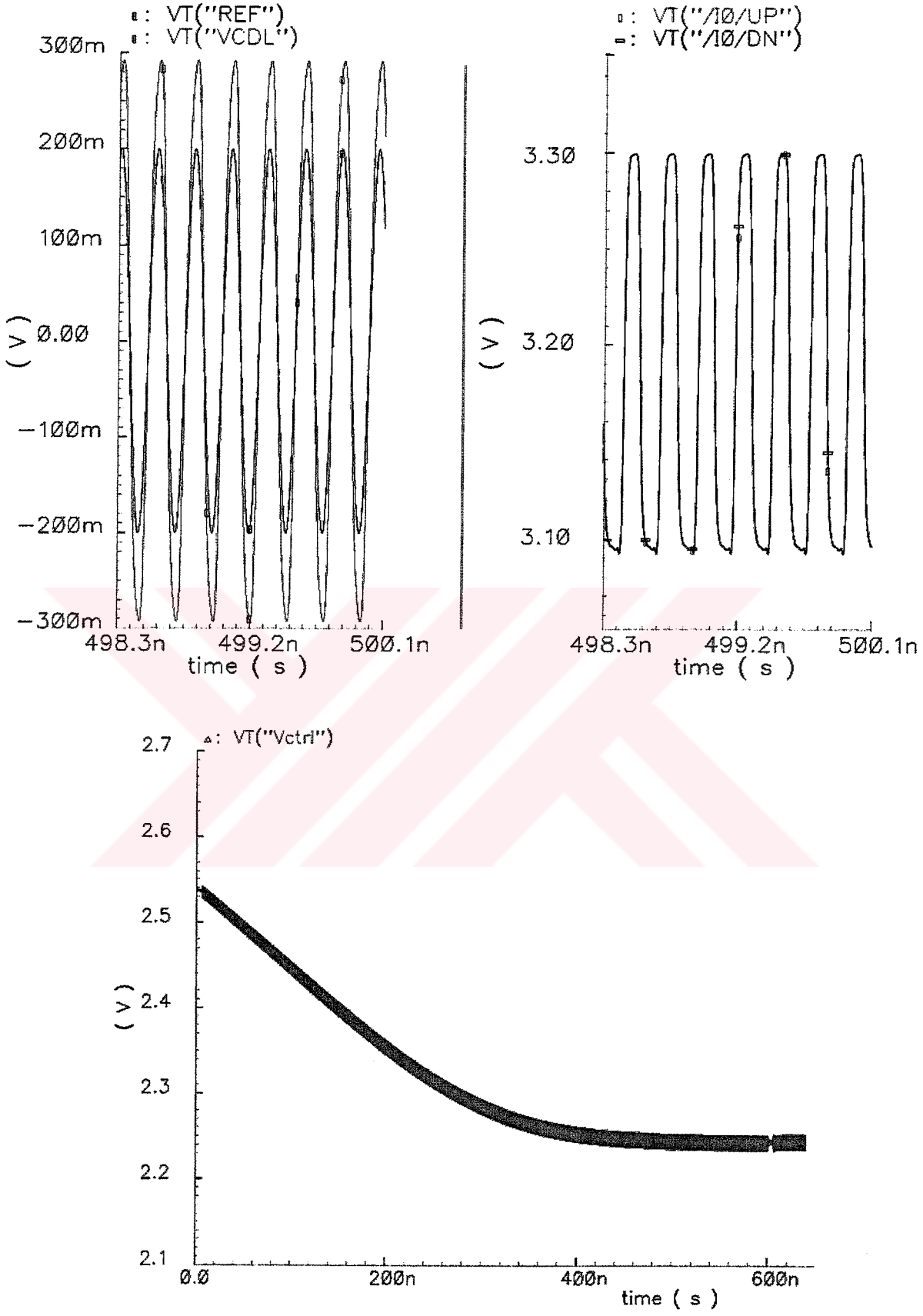


Figure 4.32 Simulation example for locked condition of DLL

5 IMPLEMENTATION & TEST

A 4GHz SiGe HBT DLL is designed to be used as a skew canceller (de-skew buffer). Design procedure that is developed during the implementation of the DLL, involves the layouts and their parasitic behaviors for different layout versions is back annotated to the schematic level design in order to achieve better performances from the circuits. Having opportunity that supplied by the 4GHz DLL, frequency multiplication option is considered in order to exploit DLL excellent noise properties. Also as a personal interest, it is important to get used to circuit design strategies at 20-50GHz range. DLL core allows frequency multiplication factor of 6 and can work up to 6GHz thus synthesized clock frequency of over 30GHz is achievable. Two different edge combiner circuits that synthesize high frequency clock signals are examined and designed.

The major problem arises from transmitting synthesized high frequency clock signal (>30GHz) to the output of the IC depending on the test equipment capabilities and packaging options. This high frequency signal cannot be taken out by the standard bonding pads and standard plastic packages, because of their bandwidth limited natures. Special care is paid to the circuit level techniques that improve the bandwidth of the bonding pads such as inductive peaking with the aid of parasitic bonding wire inductance values and integrated inductance design, or tuning out the pad capacitances with impedance matching networks again with the aid of on-chip inductances or pad design. Also investigation and evaluation of high frequency packaging options are still in progress. In order to be able to test the high frequency output signal, RF pads are designed, but insufficient testing equipment capabilities force us to develop some indirect measurement techniques. These works, which are in progress, prevents the finalization of the prototype implementation, which will make the top-level changed depending on the different requirements of each possible solution although core DLL layout design is finalized.

The following sections describes the master bias scheme of the possible prototype IC, edge combiner circuits and their output buffers and testing procedure of a stand alone VCDL which is implemented with 0.35 BiCMOS process before and layout procedures that are used during the implementation.

5.1 Master Bias

References of the current sources that are used in all the circuits of the DLL are supplied from one source, in order to avoid any major biasing problems and independent circuit performances. Although resistor mismatches whole around the IC low enough, process variations can change resistor absolute values considerably. Large change in the reference current source resistors affects the circuit performances for example voltage swings of the circuits because of the changed tail currents, changed biasing conditions of the HBT devices resulting lower f_T biasing or very high I_C biasing which can put the device into Webster or Kirk regions that result very low β and f_T. Thus a more confident reference current has to be generated.

Bandgap references experience small amount of dependency to the PVT variations, because basically their nature rely on the device physics but not circuit design parameters such as area, biasing condition etc. Thus master bias circuit is designed to have the features of bandgap reference and improve them. Bandgap reference produces 1.2V and experiences ignorable amount of change under extreme PVT conditions. The constant voltage level, 1.2V, can used to generate a desired amount of current by applying it to a properly chosen resistor.

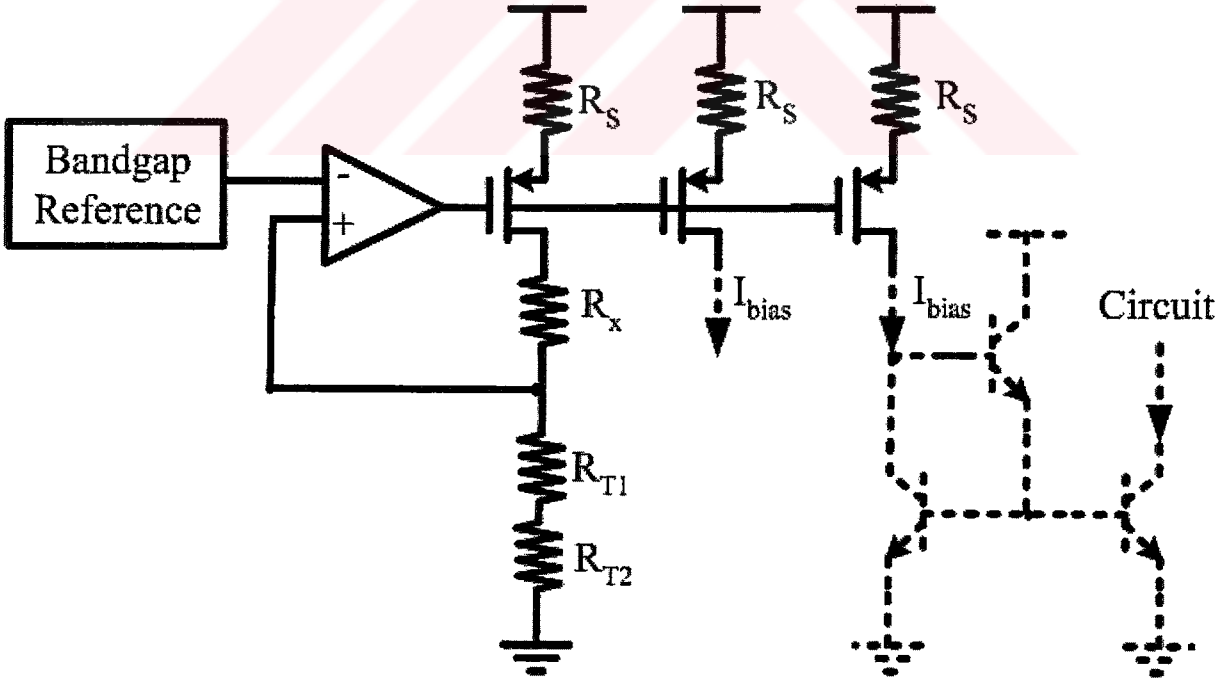


Figure 5.1 Master bias circuit.

Figure 5.1 shows master bias circuit schematic. Bandgap reference output voltage (1.2V) is applied to a resistor with an operational amplifier (OPAMP). OPAMP keeps the voltage value

over the resistor constant for all conditions by adjusting gate voltage of the PMOS transistor, which is placed at the output of the OPAMP. Thus allows constant amount of current flowing through the resistor. The reference current can be written as $I_{ref}=1.2V/R_{ref}$. The output of the operational amplifier is applied to two more PMOS transistor in order to copy the resistor current. Reference resistor is implemented with two different resistors which have opposite signed temperature coefficients ($R_{ref}=R_{T1}+R_{T2}$), in order to compensate temperature dependency of the reference current.

The absolute reference resistor value can be changed under process variations. Thus reference current changes in the opposite direction and with the aid of master bias circuit, this current compensates the changed load resistor values (changing value can have almost same percentage with the reference resistor.) of the interested circuits. Thus this feature keeps I×R products (voltage swings) of the circuits almost constant. R_x resistor is placed between the drain node of the reference PMOS transistor and the positive input of the operational amplifier in order to equalize drain node voltages of the PMOS transistors. R_s resistors improves matching of the copied currents to the reference.

Master bias circuit does not experience perfect performance but it satisfies more important demands with first order analyses. Especially temperature variations compensation of the voltage swings is vital for the VCDL.

5.2 Edge Combiner

In order to exploit DLL features, frequency multiplier circuits are concerned. There are a couple of different edge combiner circuits demonstrated in the literature but these techniques can be classified in two categories, one is the techniques rely on digital logic functions [Foley, 2000 and Zhuand, 2003] and the other is the analog approaches such as LC tank [Chien, G., 2000] or LC filtering [Spataro, A. and Deval, Y., 2003].

The work on progress that determining the final DLL which is dictated by the chosen edge combiner topologies requirement result from testing point of view that is whether determining the number of delay stages equal to either ten or twelve. In this work two different edge combiner circuits designed in comparable approach, an LC tank and a digital function those is described in following sections.

5.2.1 Digital Edge Combiner

Various logical function examples of edge combiners have been take place in the literature in recent years. Generally achieved frequency multiplication factors are F=N/2 where N is the number of delay stages and also F=N cases are valid.

For F=N/m=10/2=5 as a starting point (m=2 comes from implementation problems describing number of cycles to be locked and should not be confused with the situation described above F=N/2), odd number of equally divided phases are available from the VCDL. A logical function can be written according to Figure 5.2. For ten stage VCDL, naturally, first tap is equal to sixth tap, second tap is equal to seventh tap and so on. Thus this feature can be used for properly manage the loading conditions of each circuit. Properly combining the above waveforms can result the multiplication factor equal to F=5. The logical function can be written as,

$$x_1 = \phi_1 + \phi_3 \tag{5.1a}$$

$$x_2 = \phi_2 + \phi_4 \tag{5.1b}$$

$$x_3 = \phi_3 + \phi_5 \tag{5.1c}$$

$$x_4 = \phi_4 + \phi_6 \tag{5.1d}$$

$$x_5 = \phi_5 + \phi_7 \tag{5.1e}$$

which can be accomplished with OR gate. Starting point is VCDL tap choice that can be done according to implementation problems such as jitter performance (chapter 4.4) and loading effects. Each OR function produces a logic-0 for $T_{ref}/10$ seconds and remaining part logic-1 while having the period of T_{ref}. these resulting waveforms can be combined in order to produce logic-1 for $T_{ref}/10$ seconds and logic-0 for $T_{ref}/10$ seconds, resulting a signal having a period of $T_{ref}/5$.

$$out = x_1 \cdot x_2 \cdot x_3 \cdot x_4 \cdot x_5 \tag{5.2}$$

which is an AND gate producing an output frequency of $5 \times f_{ref}$.

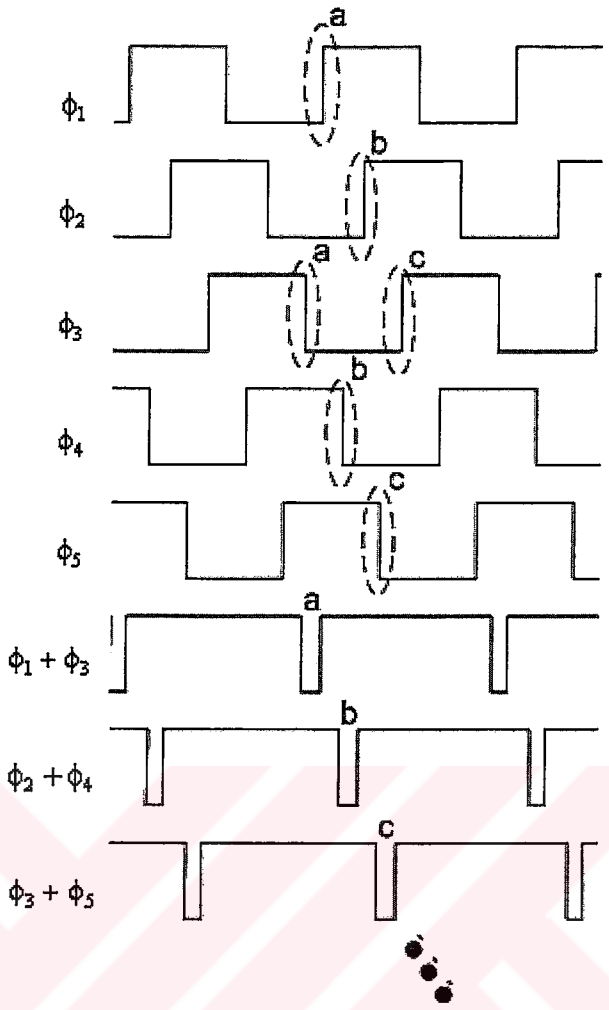


Figure 5.2 Digital edge combiner operation

It should be noted that, achieved logical function is valid for odd number of equally divided phase shifted signals. At even number of phase case, for example 6, this function can only produce $3\times f_{ref}$. Because logic-0 time reduces to $T_{ref}/6$ that can be readily seen drawing the waveforms for that case, after OR operation.

OR gates is implemented with the topology that is given in Figure 4.4 used in PFD. The problem arise from although the gate inputs at 4GHz, its output carries 20GHz information. In order to reduce the pulse width variations of the OR gate which can be problematic while the AND gate producing the final output high frequency clock signal. OR gate biasing conditions can be modified in order to increase the speed but a faster topology has been used.

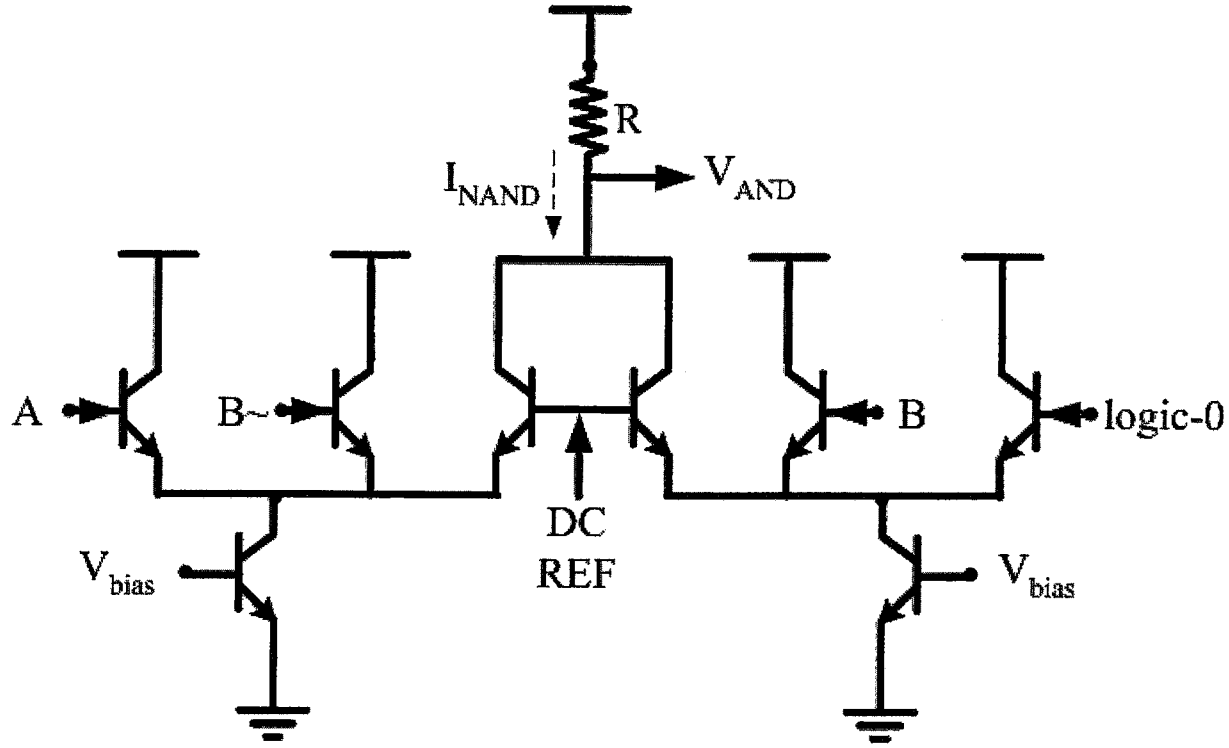


Figure 5.3 Current mode NAND gate schematic

A NAND gate has been developed from current mode EXOR gate [Razavi, B., 1994], with a little modification that can be seen in Figure 5.3. The output of the gate is its current and also with the aid of a resistor the voltage mode AND gate output can be produced. OR gate function can be done by a NAND gate.

$$F=(a+b)=(a'.b')' \tag{5.3}$$

The final AND gate function which produces multiplied output, can be accomplished with same block, but some signal conditioner blocks has to be used for proper operation. Also previous topology can be used by modifications according to F=(a.b)=(a'+b')'. Also stacked structures are developed suffering from voltage headroom problems and combined versions OR and AND gates. But current mode approaches can be more useful while the output frequency arises up to 30GHz.

As a result this edge combiner approach suffers from the higher power consumption in order to increase gate speeds. Also voltage headroom problems in case of using stacked implementations force us to use of inductors, which reduces the attractiveness of the digital operation on IC implementations.

5.2.2 LC Tank

The idea behind this approach is the summation of the equally phase shifted currents within an LC tank at proper resonance condition. Thus requires on-chip inductor component, which is not offered by the standard commercial process technologies and hard to implement in ICs because of the resistive losses to the substrate. Frankly this approach is the analog way of implementing previous edge combiner circuit.

Edge combiner time multiplexes tail currents to an LC tank according to equally phase shifted input signals (Figure 5.4). It can be shown that by properly summing delayed signals, unwanted harmonics will be ideally cancelled out at the output [Chien, G., 2000]. Thus only the synthesized output signal will remain.

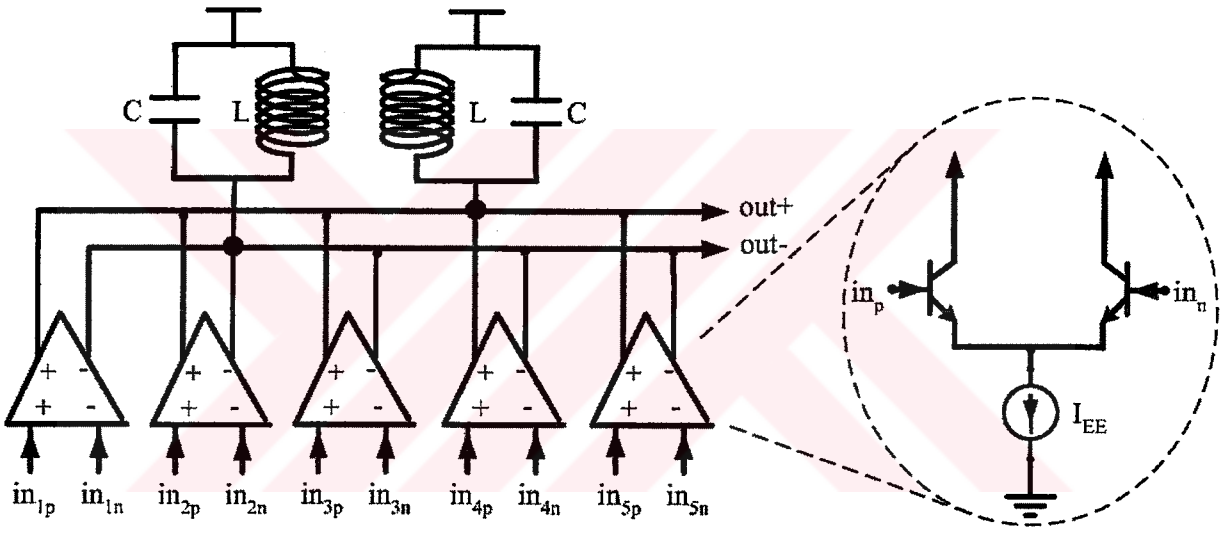


Figure 5.4 Edge combiner for five stage example with differential output

In implementation practice, inductors used to tune out the collector parasitics of the multiplexer buffer stages. Thus resonance frequency of the tank is determined by the inductor and collector parasitic capacitances. At the interested frequency range, there is no need for extra capacitance in the tank, because of the implementation problems of the inductor on chip.

For six delay stage example, only three multiplexer buffer stages are enough in order to achieve frequency multiplication factor of F=6. Because the positive outputs of second trio of the six delay stages are equal to negative ones of the first trio of the delay stages respectively. Thus only combining three delay stage differential outputs in a LC tank will result multiplication factor of six.

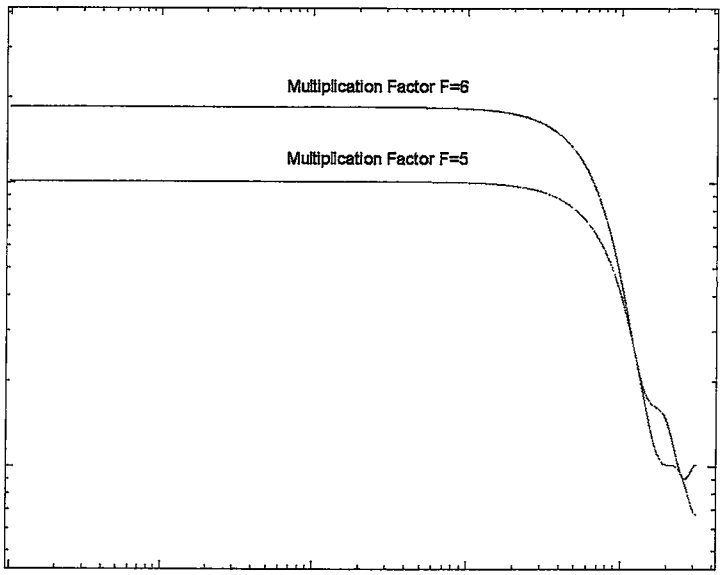


Figure 5.5 PSD plots for F=5 and F=6

In order to compare the phase noise performances for ten and twelve stage VCDL, thus achievable multiplication factors for F=5 and F=6, power spectral density functions of ideal edge combiner output is plotted according to equations (3.66) and (3.67) and jitter variances of two cases are derived from equations (4.39) and (4.40). Axes' values are not presented because of the ideal edge combining action, thus Figure 5.5 carries information for comparison point of view that is the twelve stage VCDL example output PSD is doubles the ten stage case.

The required inductor value for tuning out the collector parasitics is about 1nH at the frequency range of 20GHz–25GHz. But the configurable property of the DLL by its input frequency (4GHz–6GHz) and the number of delay stages (chosen case is 10 or12), gives us the chance of producing configurable output frequency. Thus designed inductor has a value of 0.6nH and also a varactor is placed in order to tune the resonance frequency between 20GHz to over 30GHz.

Inductor designed as having hexagonal topology with three turns at top thick metal. The radius, metal width and space are scanned in order to achieve appropriate quality factor at desired configurable resonance frequency band. Thus the highest Q is designed to be at the 25GHz with.

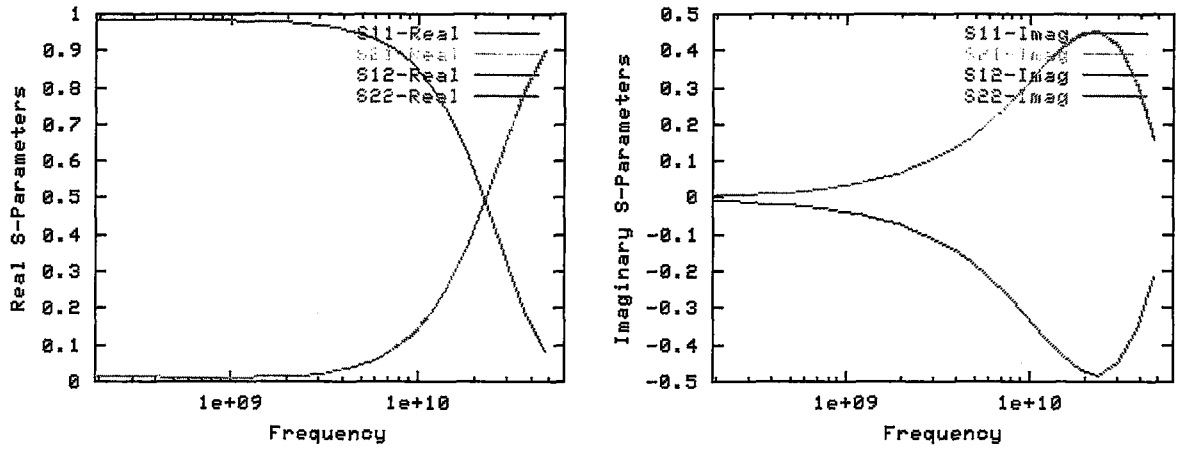


Figure 5.6 Scattering parameters of designed inductor

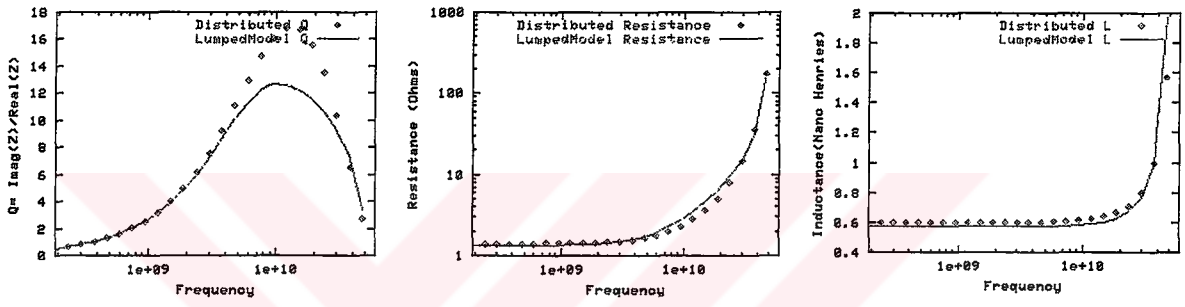


Figure 5.7 Comparison for distributed and lumped inductance models for L=600pH

Figure 5.6 shows the s-parameters of the designed inductor having value of L=600pH. Also distributed and lumped inductor models [Long, J. and Copeland, M., 1997] are compared in order to feel confident that operating frequencies at the interested range, even small metal interconnects shows inductive behavior, thus whether the required 600pH is very small that can cause some implementation problems or large enough compared to interconnect parasitic inductance values (Figure 5.7). The achieved highest Q is 12 with lumped model, the parasitic resistor is in the range of 5Ω-9Ω for 20GHz-30GHz operating frequency range. The self resonant frequency of the inductor is above 50GHz in the technology. Figure 5.8 shows the self resonant frequency of the inductor and tuned resonant frequency at the lowest value in the interested range with the aid of a varactor. Also with the aid of varactors, desired phase shift can be introduced between two different tank outputs, thus quadrature high frequency output options will be searched without modifying the core DLL building blocks.

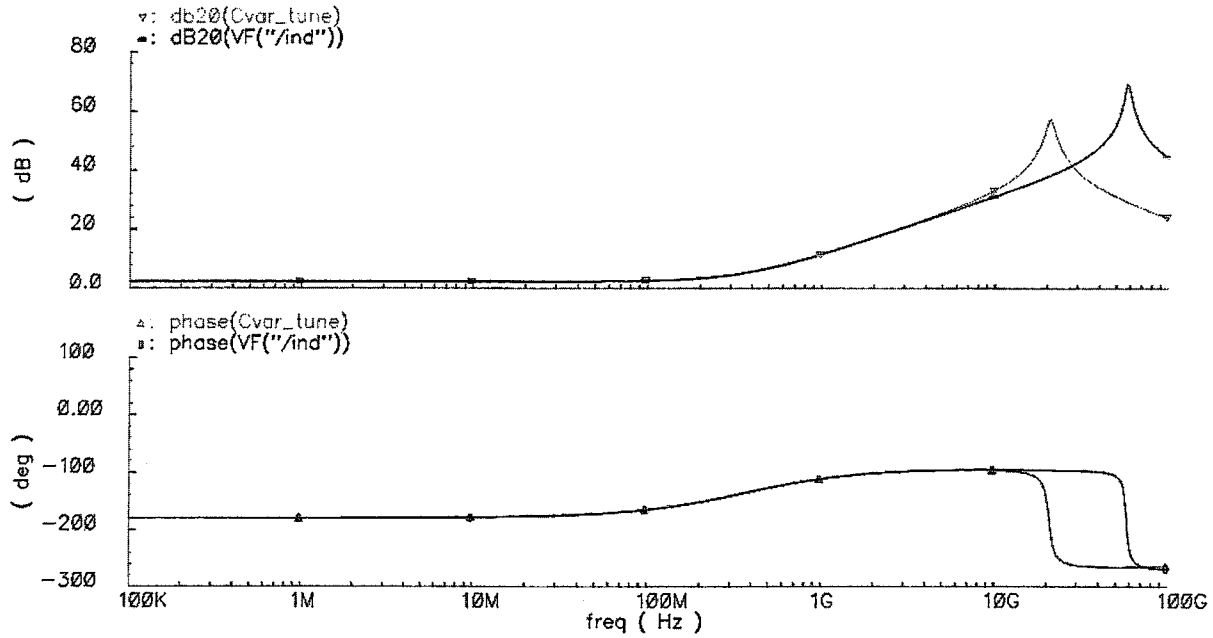


Figure 5.8 AC behavior of the inductor and inductor tuned with a varactor.

The output voltage swing of the synthesized clock signal is roughly equal to ($I_{EE}.R_{par}.Q^2$) where, R_{par} is the parasitic resistance of the inductor and Q is the quality factor. The common mode voltage level of the output signal is (V_{DD}–(a–1).$I_{EE}.R_{par}$/2) where "a" is equal to 5 in five stage example, and 3 for six stage example.

The edge combiner outputs is simulated for various cases for reference input frequency and multiplication ratios (f_{out}=F×f_{ref}), such as 5×4GHz, 6×4GHz, 5×5GHz, 6×5GHz, and 6×6GHz, either with dedicated resonant frequency with only inductor or with tuning varactor. An example case for 5×5GHz is shown in Figure 5.9, occupying an inductive peaking output buffer. The two cases are the only an inductor case and with a tuning varactor. Frequency spectrum is derived for differential outputs thus output frequency even order harmonics' levels are very low for both cases. It is obvious that varactor parasitic resistance give rise to reference frequency unwanted harmonics about 3dB compared to the inductor only case.

Also eye diagrams of the output signals are plotted for two cases in Figure 5.9; according to figure inductor only case is better. But it should be noted that the peak-to-peak jitter values shown on the figure is given in order to be able to compare the two cases, the absolute jitter values does not carries real information because device models are noiseless.

Figure 5.10 shows 6×4GHz case differential output signal.

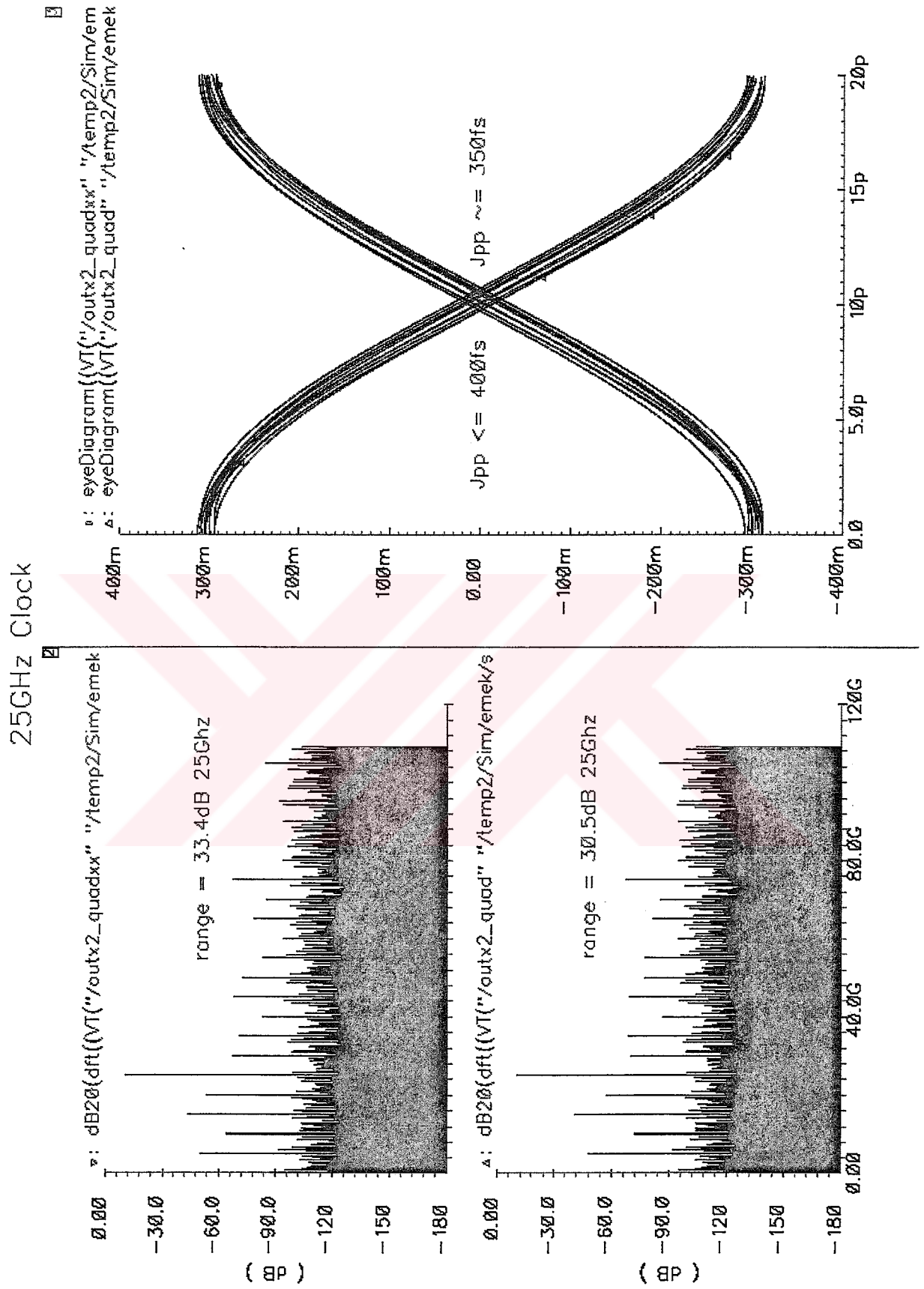


Figure 5.9 Simulation example for 5×5GHz case edge combiner output

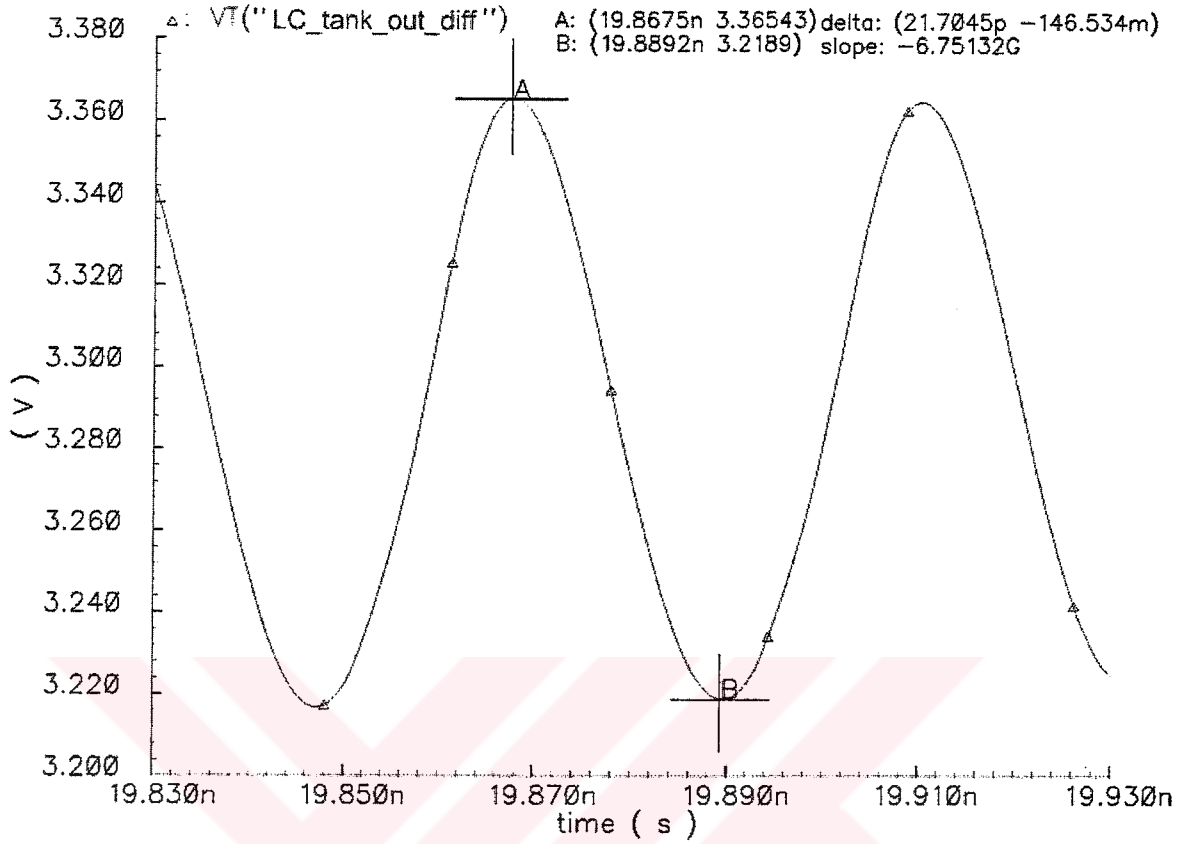


Figure 5.10 6×4GHz case LC tank differential output

5.2.3 Conclusion

In a prototype implementation two edge combiners will be compared each other with their performances. Digital edge combiner is power hungry while LC tank occupies large area. Also inductor implementation is problematic because of the losses. Thus high Q bonding wire parasitic inductance elements are planned to be used. But this time, packaging options are narrower for below 1nH parasitic inductance values (keeping in mind that 1mm bonding wire results about 1nH [Qi, X., 2001]). The bandwidth limitations of standard bonding pads which will be carrying the signal out of the IC is problematic, which can be resolved with pad design but ESD protection could be problematic because of the diode capacitances.

Thus special techniques has to be used in output buffer, such as inductive peaking or various inductor techniques [Rein, 1996 and Galal, 2003 and Lee, 2003] or wideband tuning of the pads [Galal, 2003 and Lee, 2004]. These works and also pad design is in progress with comparable approach.

5.3 Test and Measurement

Test plan for different building blocks are generally defined in relevant sections, thus this section has top-level point of view.

5.3.1 Fabricated Stand-alone VCDL

Previously a stand alone VCDL and ring oscillator VCO has been fabricated in a test chip. VCDL incorporates twelve delay stages which has the same topology given in Figure 4.20 with accumulation mode varactors having different tuning ranges. Also emitter followers are not occupied. The aim of the implementation of the VCDL is to determine the noise behavior. Also ring oscillator configuration of the VCDL, which is built up with same number of delay stages and topology sharing the control signal.

Ring oscillator does not give direct information for VCDL noise properties because of jitter accumulation phenomenon that experiences. But indirect measurement techniques can be used. The aim of Ring oscillator is to determine the control voltage versus delay characteristics of the VCDL. It is well known that, ring oscillator output frequency is,

$$f_{vco}=1/(2.N.T_{dps}) \tag{5.4}$$

where N is the number of delay stages, and T_{dps} is the delay per stage. Thus according to above relationship, ring oscillator VCO, can help us to determine the VCDL delay characteristics for different control voltage levels. This characteristic of the VCDL is hard to derive at 4GHz in picoseconds resolution that requires high capability testing equipment and may be impossible to achieve.

Thus VCDL is used to determine the phase noise and jitter characteristics and VCO is used to characterize the VCDL delay versus control signal. Also control voltage noise immunity can be tested.

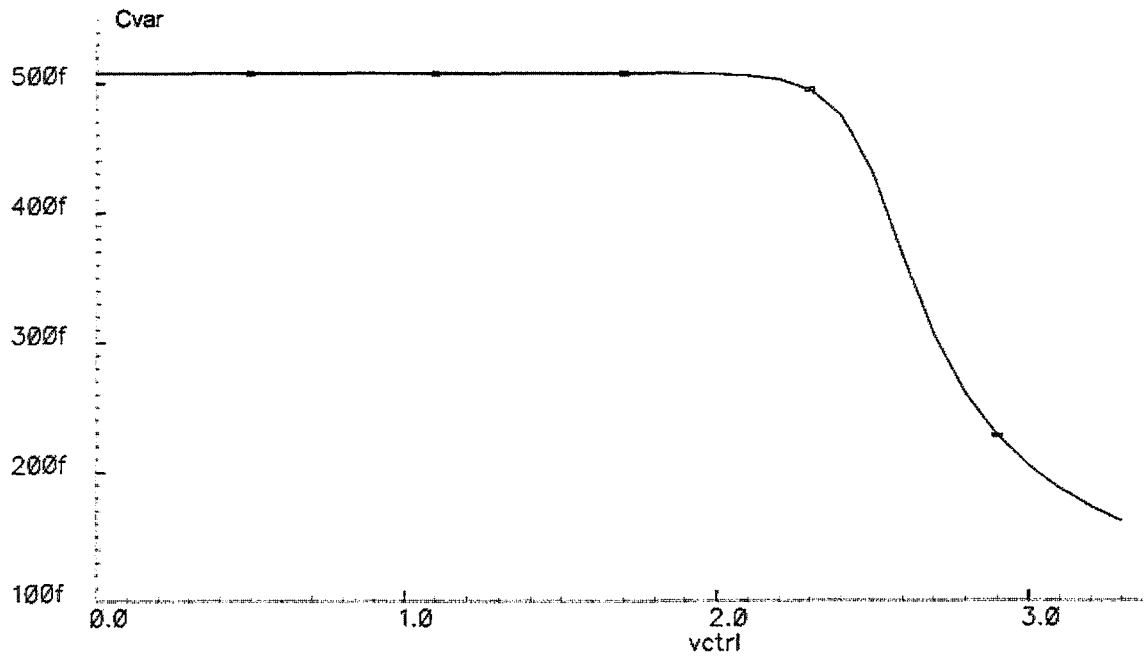


Figure 5.11 Varactor tuning curve used in fabricated VCDL

The fabricated VCDL and VCO delay stages uses different accumulation mode varactors that are used in the final core DLL design. Varactors tuning curve is given in Figure 5.11, which has lower C_{max} and C_{min} values, thus resulted minimum/maximum stage delays are lower than the used delay stage in chapter 4. These values are used because VCDL has been considered for only skew cancellation application thus there are no any additional loads for each delay stage but the following ones.

The resulted oscillation frequency for VCO for two extreme control voltage cases are about 560MHz (T=1/f=1.77ns) and 840MHz (T=1.19ns). From equation (5.4) minimum delay per stage is calculated about to be 50ps and 75ps for maximum case. Thus total minimum/maximum delay of the VCDL becomes at around 590ps and 880ps respectively.

The characterization measurements of the stand alone VCDL and VCO are in progress, which will give useful information that will be used for newly designed core DLL and test circuits. Figure 5.12 shows die photo of stand alone VCDL and VCO. VCDL differential output is taken to the RF-pads with current starving buffer stages, in order to estimate the noise performance of them.

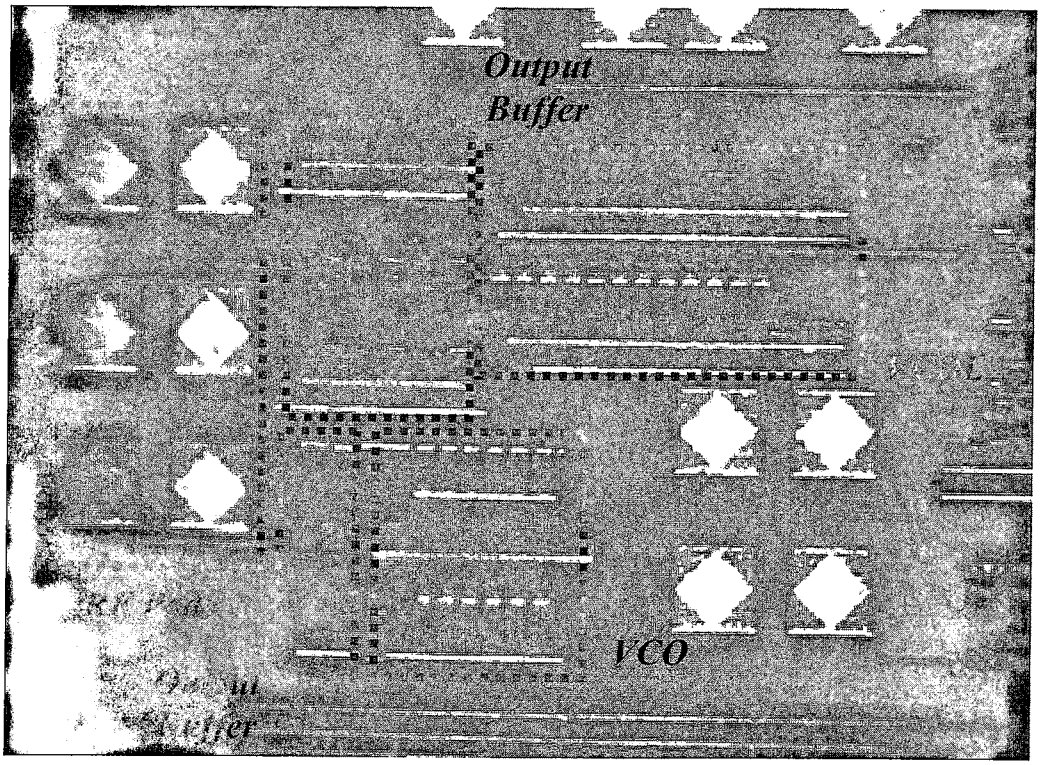


Figure 5.12 Stand-alone VCDL and VCO die photo

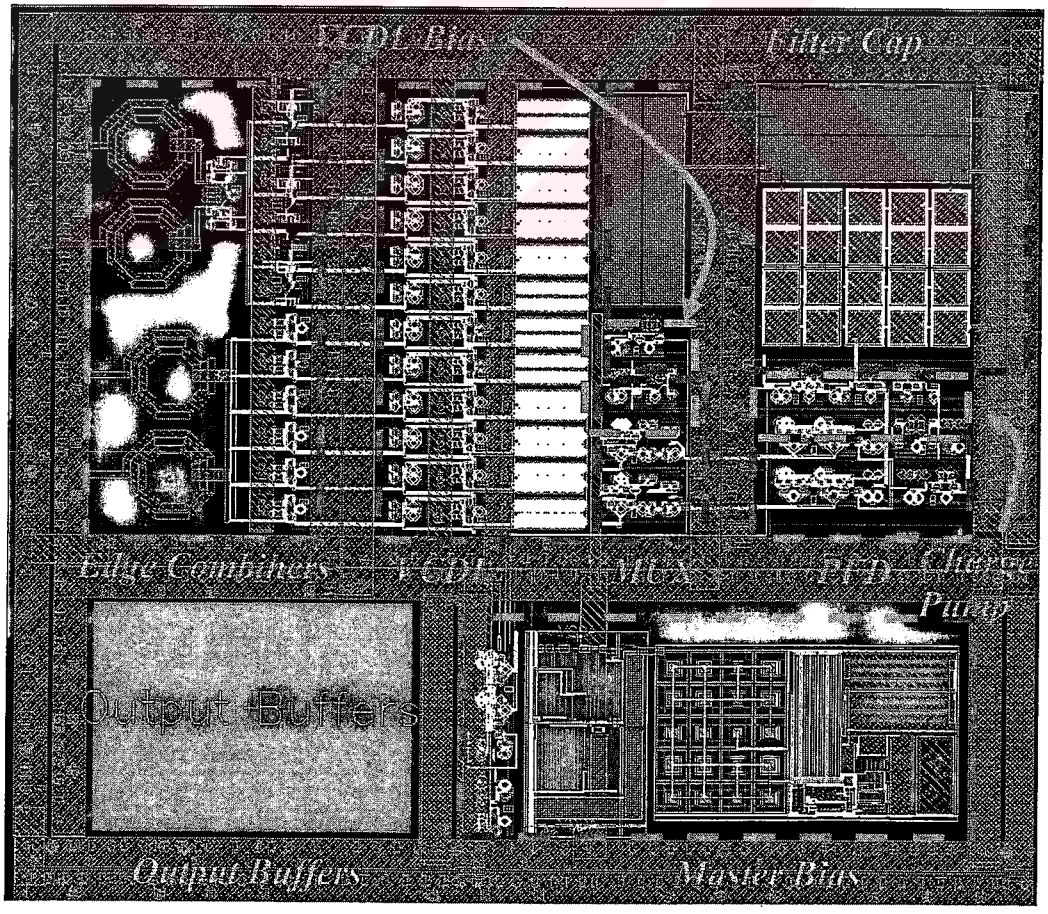


Figure 5.13 Prototype IC toplevel layout

5.3.2 Prototype IC

Figure 5.13 shows top-level layout of the prototype IC. During layout some priorities has been determined such as symmetry, minimizing parasitic resistance or capacitance elements of the interconnects according to the relevant circuits' operation and the thermal gradient whole over the IC. Also parasitic capacitance value between the supply rails has been increased with the aid of multilayer power grid in order to increase the coupling, which increases immunity to the V_{DD}/Ground bounce problems. Differential signal lines has been drawn parametrically and parasitic extraction has been made in order to determine optimum line apertures and widths. First and second metal layers of the four available metal layers has been reserved for sub-blocks interconnects, and metal-3 for high speed clock signal lines and widen top thick metal layer for power routing. Also other metal layers have been used for power routing in order to reduce the I×R drop further. Except output buffers design has been finalized but according to output buffer specifications edge combiner circuitries' layouts may differ from the given form. Total die area is below $1mm^2$ and core DLL die area becomes almost $0.55\times0.5mm^2$.

In order to have testing ability, DLL loop bandwidth is adjustable with externally variable charge pump current as mentioned in chapter 4. Also loop filter capacitor is partially implemented with high-Q MIM capacitors (30pF) and high density stack capacitors (70pF, 80pF and 90pF) in order to have more loop bandwidth tuning range. Besides capacitor occupies large silicon area, thus external filter can be placed, which will allow us to use different order loop filters for "phase filtering [Edward Lee, 2003]" according to measured phase noise profile of the DLL and manipulate the jitter transfer characteristics.

Frequency multiplying edge combiner circuits will be measured also. LC tank varactors can be tuned externally, in order to change the resonant frequency according to multiplication ratio. Also varactor tuning will allow us to adjust tank phase responses, which can be used to achieve phase shifted output signals for two LC tanks. Additional stand-alone inductors and varactors are planned to be characterized. Measurement equipment capabilities will also contribute to test planning.

Besides DLL functionality, the most important measurement will be done is the jitter performance of the DLL, which will guide us to verify the calculated jitter performance in section 4.4. Also frequency multiplier DLL configuration performance will be characterized. The DLL configurations and each independent block selection for measurement will be done

by controlling the 2:1 multiplexer circuit, which routes the tenth or twelfth delay stage output to the phase/frequency detector and master bias with additional control inputs added to the given topology in section 5.1 that can power-up the each sub-block by enabling or disabling the relevant reference current sources.

Figure 5.14 shows designed prototype DLL functional chip overview. Except the edge combiners and their output buffers, the prototype design is finalized (these blocks are highlighted with dashed dot lines). The major testing problem arises from bandwidth limitations of the bonding pads for the multiplied frequency range as mentioned in previous section. Thus, edge combiner outputs will be observed with RF-pads also.

Final top-level floor-plan of the prototype IC might be changed according to the package selection, choice of the solution for output pads bandwidth problems, thermal gradient whole over the IC that which would be affected by the chosen solutions and testing equipment capability enhancements operating up to 30GHz which are planned to be done till the end of the summer of 2004. Also detailed test planning will be done according to measurement equipment park.

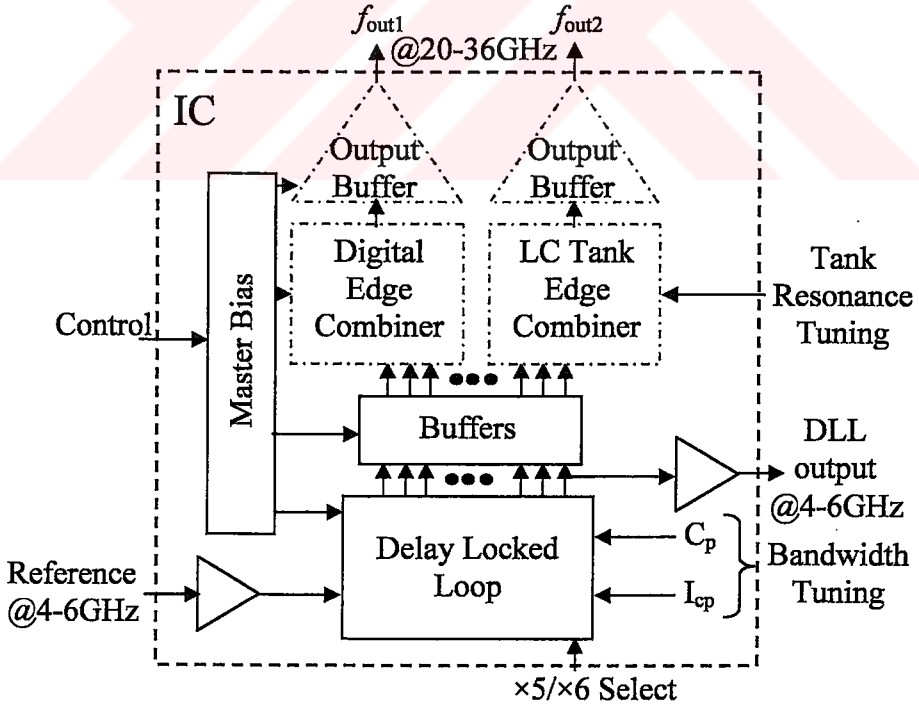


Figure 5.14 Prototype IC block diagram

REFERENCES

Andreani, P. and Matisson, S., 2000. "On the Use of MOS Varactors in RF VCO's", IEEE Journal of Solid-State Circuits, vol.35, no.6.

Bilotti, A., and Mariani, E., 1975. "Noise characteristics of current mirror sinks/sources," IEEE Journal of Solid-State Circuits, vol. SC-10, no. 6, pp. 516-524.

CADENCE., 2001. Oscillator Noise Analysis in SPECTRE-RF, CADENCE.

CADENCE., 1998. Modeling and simulation of jitter in PLL frequency synthesizers.

Chien, G., 2000. "Low Noise Local Oscillator Design Techniques using a DLL-based Frequency Multiplier for Wireless Applications", Ph.D. Thesis, University of California, Berkeley.

Comstron., 1995. Phase Noise Theory and Measurement Application Note, Areoflex.

Edward Lee, M. and Dally, W. and Greer, T., 2003. "Jitter Transfer Characteristics of Delay-Locked-Loops – Theories and Design Techniques", IEEE Journal of Solid-State Circuits, vol. 38, no.4.

Freidman, H. and Meghelli, M., 2003. "SiGe BiCMOS Integrated Circuits for Highspeed Serial Communication Links", IBM J. RES. & DEV. vol.47 no. 2/3.

Foley, D. and Flynn, M., 2000. "CMOS DLL Based 2V, 3.2ps Jitter, 1GHz Clock Synthesizer and Temperature Compensated Tunable Oscillator", in Proc. of CICC, pp. 371-374, May.

Fong, N. and Kim, J. and Plouchart. J., 2004. "A Low-Voltage 40-GHz Complementary VCO With %15 Frequency Tuning Range in SOI CMOS Technology", IEEE Journal of Solid-State Circuits, vol.39, no.5.

Galal, S. and Razavi, B., 2003. "Broadband ESD Protection Circuits in CMOS Technology", IEEE Journal of Solid-State Circuits, vol.38, no.12.

Galal, S. and Razavi, B., 2003. "10-Gb/s Limiting Amplifier and Laser/Modulator Driver in 0.18-μm CMOS Technology", IEEE Journal of Solid-State Circuits, vol.38, no.12.

Gardner, F., 1980. Charge-pump Phase-Locked Loops, IEEE Trans. Comm., vol. 28, pp. 1849-1858.

Gray, P. R., and R. G. Meyer, 1984. "Analysis and design of analog integrated circuits." New York: Wiley.

Hajimiri, A. and Lee, T., 1999. " Jitter and Phase Noise in Ring Oscillators", IEEE Journal of Solid-State Circuits, vol.34, no.6.

Hegazi, E. and Abidi, A., 2003. "Varactor Characteristics, Oscillator Tuning Curves, and AM-FM Conversion", IEEE Journal of Solid-State Circuits, vol.38, no.6.

Johansson, H., 1998. "A Simple Precharged CMOS Phase Frequency Detector", IEEE Journal of Solid-State Circuits, vol. 33, no.2.

Johnson, M. and Hudson, E., 1988. "A Variable Delay Line PLL for CPU-Coprocessor Synchronization", IEEE Journal of Solid-State Circuits, vol. 23, pp. 1218-1223.

Kim, B. and Weigandt, C. and Gray, P. 1994. "PLL/DLL System Noise Analyses for Low Jitter Clock Synthesizer Design", –.

Kishine, K. and Kobayashi, Y. and Ichino. H., 1997. "A High-Speed Low-Power Bipolar Digital Circuit for Gb/s LSI's: Current Mirror Control Logic", IEEE Journal of Solid-State Circuits, vol.32, no.2.

Lee, J. and Razavi, B., 2003. "A 40-Gb/s Clock and Data Recovery Circuit in 0.18-μm CMOS Technology", IEEE Journal of Solid-State Circuits, vol.38, no.12.

Lee, J. and Huh, Y., 2004. "Design of ESD Power Protection With Diode Structures for Mixed-Power Supply Systems", IEEE Journal of Solid-State Circuits, vol.39, no.1.

Lee, T. and Hajimiri, A., 2000. " Oscillator Phase Noise: A Tutorial", IEEE Journal of Solid-State Circuits, vol.35, no.3.

Liu, A. and Lee, J. and Tsao, H., 1999. "Low-Power Clock-Deskew Buffer for High-Speed Digital Circuits", IEEE Journal of Solid-State Circuits, vol. 34, no.4.

Long, J. and Copeland, M., 1997. "The Modelling, Characterization, and Design of Monolitic Inductors for Silicon RF IC's", IEEE Journal of Solid-State Circuits, vol.32, no.3.

Maneatis, J., 1996. "Low Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE Journal of Solid-State Circuits, vol. 31, no. 11, pp. 1723-1731.

McNeill, J.A., 1994. "Jitter in Ring Oscillators", Ph.D. Thesis, Boston University.

McNeill, J. A., 1997. "Jitter in Ring Oscillators", IEEE Journal of Solid-State Circuits,

vol.32, no.6, pp. 870-9.

Murata, K. and Sano, K., 2004. "100-Gb/s Multiplexing and Demultiplexing IC Operations in InP HEMT Technology", IEEE Journal of Solid-State Circuits, vol.39, no.1.

Nielsen, S. and Yen, J., 2003. "A Fully Integrated 43.2-Gb/s Clock and Data Recovery and 1:4 Demux IC in InP HBT Technology", IEEE Journal of Solid-State Circuits, vol.38, no.12.

Ong, A. and Benyamin, S., 2003. "A 40–43-Gb/s Clock and Data Recovery IC With Integrated SFI-5 1:16 Demultiplexer in SiGe Technology", IEEE Journal of Solid-State Circuits, vol.38, no.12.

Pak, B., 2002. "2.4GHz CMOS PLL Frequency Synthesizer", Ms. Thesis, Istanbul Technical University.

Paulino, N. and Serrazina, M., 2003. "Design of a Digitally Programmable Delay-Locked-Loop for a Low-cost Ultra Wide Band Radar Receiver", IEEE

Qi, X., 2001. "High Frequency Characterization and Modeling of on-chip Interconnects and RF-IC Wire Bonds" Ph. D. Thesis, Stanford University

Ramin, F. and Dally, W., 2002. "A Low-power Multiplying DLL for Low-Jitter Multigigahertz Clock Generation in Highly Integrated Digital Chips", IEEE Journal of Solid-State Circuits, vol. 37, no.12.

Razavi, B. and Ota, Y. and Swartz. R., 1994. "Design Techniques for Low-Voltage High-Speed Digital Bipolar Circuits", IEEE Journal of Solid-State Circuits, vol.29, no.3.

Razavi, B., 1995. "Principles of Data Conversion System Design", IEEE Press.

Razavi, B., 1998. "RF Microelectronics", IEEE Press.

Razavi, B., 2002. "Challenges in the Design of High-Speed Clock and Data Recovery Circuits", IEEE Communication Magazine, August.

Regis, M. and Borgarino, M., 2000. "Non-linear Noise Mechanisms in SiGe BiCMOS Devices", IEEE.

Rein, H. and Moller, M., 1996. "Design Considerations for Very-High-Speed Si-Bipolar IC's Operating up to 50 Gb/s", IEEE Journal of Solid-State Circuits, vol.31, no.8.

Rogers, J. and Long, J., 2002. "A 10-Gb/s CDR/DEMUX With LC Delay Line VCO 0.18-μm CMOS", IEEE Journal of Solid-State Circuits, vol.37, no.12.

Shanmugan, K. S., and A. M. Breipohl, 1988. "Random signals: detection, estimation, and data analysis." New York: Wiley.

Spataro, A. and Deval, Y., 2003. "A VLSI CMOS Delay Oriented Waveform Converter for Polyphase Frequency Synhtesizer", IEEE

Suzuki, A. and Kawahito, S., 2002. "A Digitally Skew Correctable Multi-phase Clock Generator using a Master-Slave DLL", IEEE

van de Beek, R. and Klumperink, E., 2002. "On Jitter Due to Delay Cell Mismatch in DLL-Based Clock Multipliers", IEEE.

Van Haaren, B. and Regis, M., 1998. "Noise Properties of SiGe Heterojunction Bipolar Transistors", IEEE.

Verhoeven, C. J. M., "First order oscillators," Ph. D. Thesis, Delft University.

Walden, R.H., 1999. "Analog-to-Digital Converter Survey and Analysis", IEEE Journal of Selected Areas in Communications, vol. 17, no.4.

Weigandt, C. and Kim, B. and Gray, P. 1994. "Timing Jitter Analysis for High-Frequency, Low-Power CMOS Ring-Oscillator Design", ISCAS, June, 1994.

Weigandt, C., 1998. "Low-Phase-Noise, Low-Timing-Jitter Design Techniques Delay Cell Based VCOs and Frequency Synthesizers", Ph.D. Thesis, University of California, Berkeley.

Ye, S. and Jansson, L. and Galton, I., 2003. "Techniques for In-band Phase Noise Suppression in Re-circulating DLLs", IEEE Custom Integrated Circuit Conference

Zhuand, J. and Du, Q., 2003. "A -107dBc, 10KHz Carrier Offset 2-GHz DLL-Based Frequency Synhthesizer", IEEE Custom Integrated Circuit Conference

BIOGRAPHY

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